Phase-Locked Loops
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Lecture – 12
Frequency Acquisition Limits in Type–I PLLs

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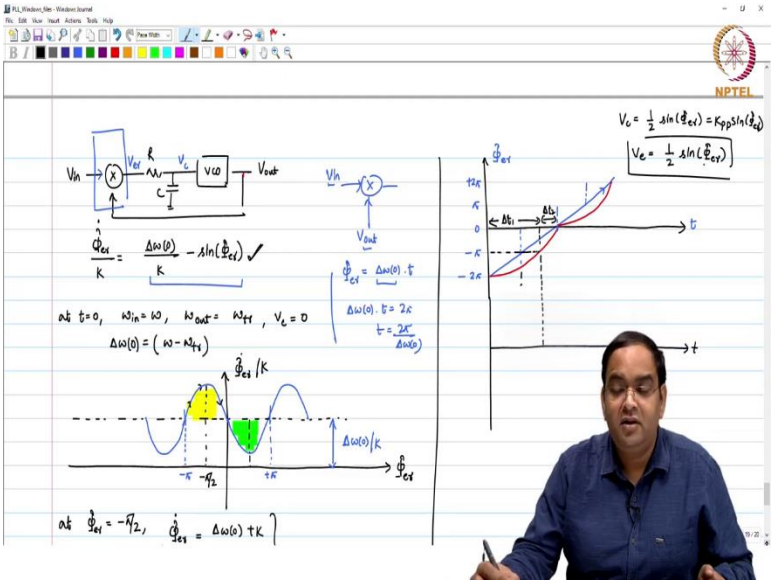

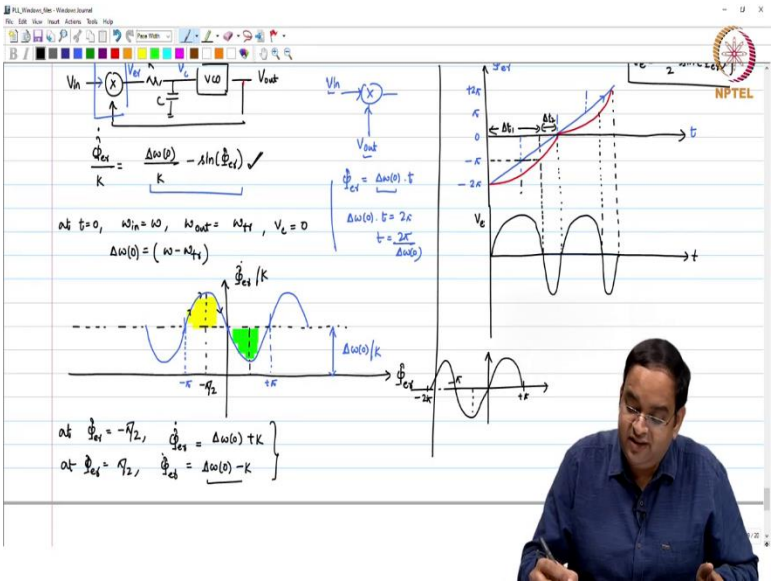

In the previous session, we looked at the locking in Type-I PLL and we found the stable solutions while defining $\frac{\dot{\varphi_{er}}}{K}$. So, let me just quickly recall what we have looked at. So, this was our Type-I

PLL with R and C and VCO connected in feedback, these are V_{in} and V_{out}. What we have observed is that we tried to find the solution in the locked case where we were looking at the following:

$$\frac{\dot{\varphi_{er}}}{K} = \frac{\Delta\omega(0)}{K} - \sin(\varphi_{er})$$

If this equation has a solution, then the PLL locks, otherwise the PLL does not lock. Now, a question arises that if the PLL does not lock, then, what does it do? You give the input signals and you have an initial frequency error. So, we have,

$$\text{At } t = 0,\ \omega_{in} = \omega,\ \omega_{out} = \omega_{fr},\ V_c = 0$$

So, you have $\frac{\dot{\varphi_{er}}}{K}$ which is given above and you have frequency error at the beginning.
So, $\Delta\omega(0)$ is given by,

$$\Delta\omega(0) = \omega - \omega_{fr}$$

If this frequency error is large, the PLL does not lock. The question is what does it do? So, let us figure out what it does. So, I will plot the same thing for the case when you do not have a solution for this equation. So, let us see this, you have φ_{er} here and this one is $\frac{\dot{\varphi_{er}}}{K}$ and assuming that there is no solution, I will plot it.

So, this is the kind of waveform you have. The blue curve is nothing but what you see on the right-hand side of the above equation. You do not see the blue curve crossing the x-axis at all, and this is nothing but $\frac{\Delta\omega(0)}{K}$. Well, it does not cross the x-axis, that is fair enough, no problem with that. What does it do? To figure out that, let us note these points. So, this is $-\pi$, this is $+\pi$.

So, if I connect everything in the PLL as shown to you here, you will have error voltage and control voltage, just that these voltages will not settle to a fixed value because it does not lock. So, what is happening here is the following. If you look at the upper part of this curve which is here, and similarly, the lower part which is here. In both these cases, what you see here is, I will just write this part, you pick up this particular point which is $-\frac{\pi}{2}$.

$$\text{At } \varphi_{er} = -\frac{\pi}{2}, \qquad \dot{\varphi_{er}} = \Delta\omega(0) + K$$

So, the rate of change of phase error with respect to time is $\Delta\omega(0) + K$. Similarly, we have,

$$\text{At } \varphi_{er} = \frac{\pi}{2}, \quad \dot{\varphi_{er}} = \Delta\omega(0) - K$$

So, the rate of change of phase error is $\Delta\omega(0) - K$. It should be noted here that K is a positive value. Now, when you start this PLL with initial frequency error, $\Delta\omega(0)$, and you do not have any solution which gives you that the rate of change of phase error is equal to zero, then the waveform will keep on changing or these voltage signals here will keep on changing and they will not settle to any fixed value.

At that particular time, what you observe from our previous analysis is that at some particular phase error or we have chosen only two points, out of these phase errors, at one particular phase error, the rate of change of phase error is maximum, and in the other case, the rate of change of phase error is minimum. $\Delta\omega(0) + K$ tells us that the rate of change of phase error is maximum whereas $\Delta\omega(0) - K$ tells us that the rate of change of phase error is minimum. So, the PLL is still running, it has not locked. The only thing is that sometimes the phase error changes slowly and sometimes the phase error changes fast. How does it matter? Let us see that. So, we will try to understand what happens here. So, for that, what I will first do is, I will show you the case, let us pick up, simplify it a little bit and consider the mixer stand-alone or the phase error detector stand-alone which is this block, phase error detector.

In this case, you are considering only the mixer part. So, I have V_{in}, I have V_{out}, and let us say this is not connected in the loop, just to understand how the phase error would have changed if there was a frequency error, but it was not in the feedback loop. If that would have been the case, the phase error would increase linearly. There is no doubt. Because if you have frequency error between these two, the phase error is given by,

$$\varphi_{er} = \Delta\omega(0).t$$

It is linear. So, I am plotting phase error with respect to time here. The blue one is for open loop. So, it may start from -2π, goes to $-\pi$, then 0, then $+\pi$, $+2\pi$ and it is going to get all these values at fixed intervals of time and these fixed intervals of time depend on $\Delta\omega(0)$.

So, we have,

$$\Delta\omega(0).t = 2\pi$$

$$t = \frac{2\pi}{\Delta\omega(0)}$$

So, you are going to accumulate this phase error in time $\frac{2\pi}{\Delta\omega(0)}$, if you start from time instant $t = 0$. That is just a reference which I chose, you can choose anything. The important part here is that for a mixer in open loop, the phase error will keep on increasing linearly.

Now, we have just analyzed that if the frequency error is larger than K, then sometimes the phase error increases slowly and sometimes the phase error increases in a fast manner. So, both the things will happen. We have seen that the rate of change of phase error when the phase error is $-\frac{\pi}{2}$ is faster and when the phase error is $+\frac{\pi}{2}$, it is slower. And this rate of accumulation of the phase error is periodic in nature. Whatever is happening in one period, the same thing is going to happen in the other period.

So, if we look at the phase error in the closed loop or in the loop where we are having V_{out} affecting the mixer input, what we will see is that the phase error may start from some value and then it increases slowly and then it may lead to zero here. Every 2π, it is going to repeat this. It is not going to increase linearly. While plotting this red curve, I have assumed that control voltage is equal to error voltage. So, in this red plot, my assumption is given below.

$$V_c = V_e$$

We know that the error voltage is given by,

$$V_e = \frac{1}{2}\sin(\varphi_{er})$$

Thus, we have,

$$V_c = \frac{1}{2}\sin(\varphi_{er}) = K_{PD}\sin(\varphi_{er})$$

Only when I assume this, the output frequency will change and based on the output frequency, we have already derived this equation.

The thing which we are not proving by writing the exact expression, we are just using these two and saying because sometimes the phase error increases slowly and at other times it increases fast, the change in the phase error which you will see will not be linear with respect to time from -2π

to 0. So, it will be non-linear. So, in this particular case what you see is that it accumulates phase from -2π to π in larger time. If I call this as Δt_1, then, Δt_1 is larger than Δt_2, this is what we are talking about.

So, if such is the phase error accumulation, then, in response to this phase error, what is the error voltage? The error voltage is $\sin(\varphi_{er})$. If the error voltage is $\sin(\varphi_{er})$, then, what is the error voltage for the case when the phase error is not changing linearly and it always keeps on going from -2π to 0 and 0 to 2π, it keeps on increasing but with a different rate of change. So, for this particular case, you understand that the error voltage is nothing but $\frac{1}{2}\sin(\varphi_{er})$. We are rejecting the high frequency component, $\omega_{in} + \omega_{out}$, that is something which we have been neglecting so far. So, let us neglect that and only focus on this error voltage.

So, if I just plot the sine waveform, we all know that the sine waveform is nothing but this. This is your sine waveform. This is $-\pi$, this is $+\pi$, this is -2π. So, when you go from -2π to $-\pi$, $\frac{1}{2}\sin(\varphi_{er})$ is positive, it is changing not like a sine wave but maybe some other waveform. And then during Δt_2 time, you may have this. This waveform will keep on repeating because the PLL never settles. So, this is going to repeat. Assume that the two waveforms which I drew are the same, this is what you will see as the error voltage. Now, this keeps on happening, this particular part will keep on always happening.

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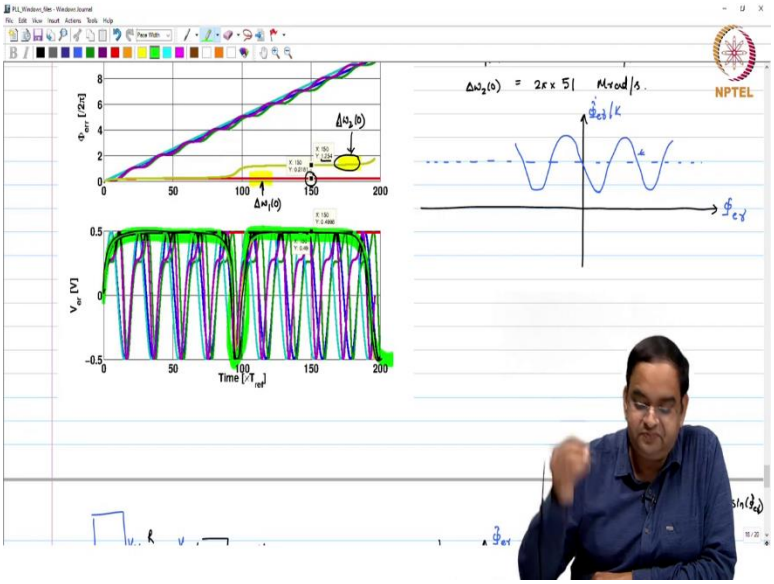

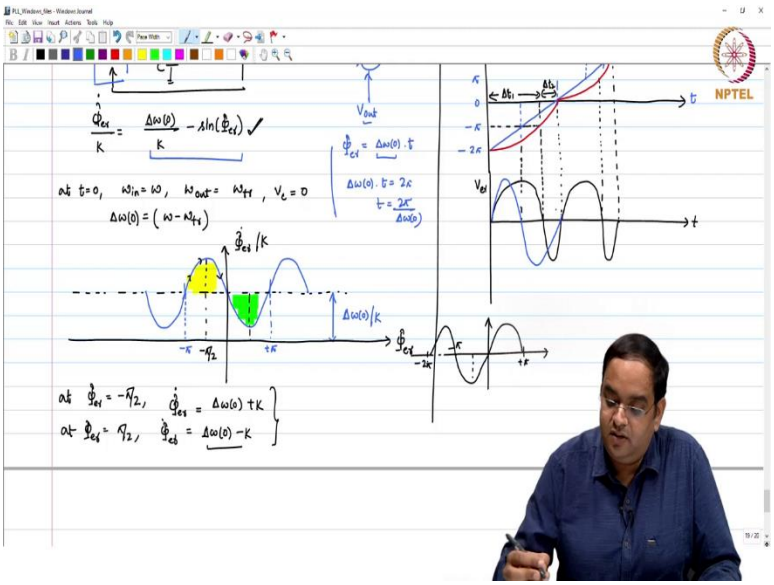

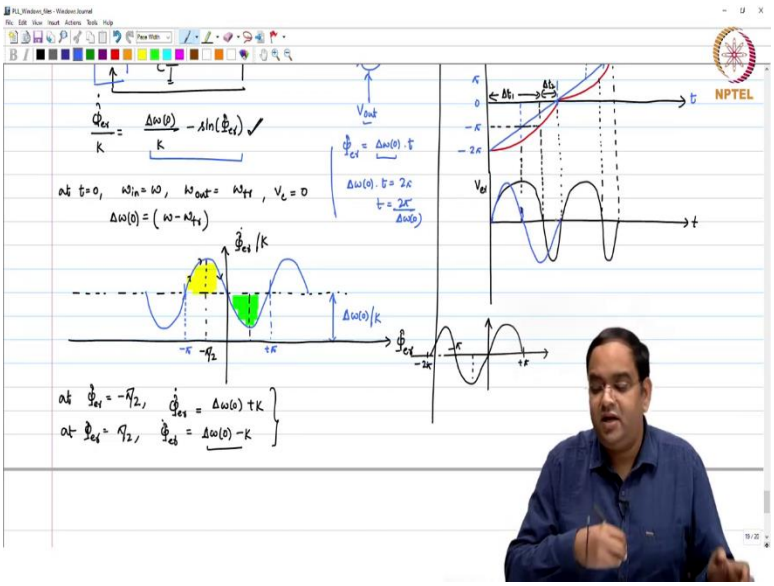

If such is the case which you see here when the PLL does not lock, this is the same thing which I did not tell previously, but I showed you that the waveform just keeps on doing something like this. And you know that this error voltage is passed as the control voltage. And when it is passed as the control voltage (V_c), even the control voltage (V_c) will do the same thing and the PLL is never going to lock.

One interesting thing which you can see is that the waveform which you are seeing here, the error voltage (V_e) waveform, it does not have a zero average voltage. In case the PLL was in open loop, then the error voltage (V_e) would just be a sinusoid. In case you have an open loop, the phase error

will be something like this. Well, on the plot you do not see this has a zero average but actually it does, this is like a sine wave and it is repeated.

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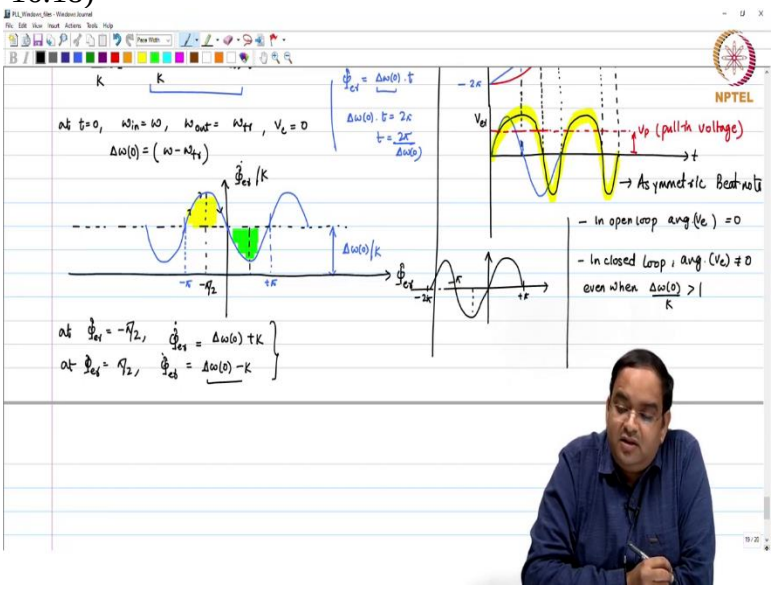

So, the difference is that in open loop, $\text{avg}(V_e) = 0$ for any given frequency error. In closed loop, $\text{avg}(V_e) \neq 0$ even when $\frac{\Delta\omega(0)}{K} > 1$. In our case, that is what I am showing you here, this is what we see here. So, if that is the case, there is some kind of information in the error voltage (V_e) about the frequency error but it will not be able to lock at all.

The DC value, the average value of this error voltage (V_e) which you see here in black, whatever that value is, is called as the pull-in voltage (V_P). There is a meaning attached to it which we will see later. So, this is the pull-in voltage. Now, the waveform which you see here is asymmetric in nature. This particular waveform is asymmetric in nature and often referred to as asymmetric beat note. It is like a beat here. It is asymmetric in nature, it has a non-zero DC voltage, that non-zero DC voltage is called as pull-in voltage. So, what can we do with this pull-in voltage, that is something which we need to see. Thank you.