Introduction to Semiconductor Devices

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Module No # 13

Lecture No # 66

Threshold Voltage Characteristics of Short Channel MOSFET

Hello everyone welcome back to introduction to semiconductor devices in the previous video we spoke about the short channel effects. We discussed how the reduction of channel length will influence the current characteristics of a MOSFET and these are the very important because I think about 2000 or so we have entered into the short channel regime. And now most of the MOSFET are actually short channel MOSFET and it is important to understand them in detail.

So now today this video the emphasis will be to understand the impact of shorter channel length on the V_T of a MOSFET.

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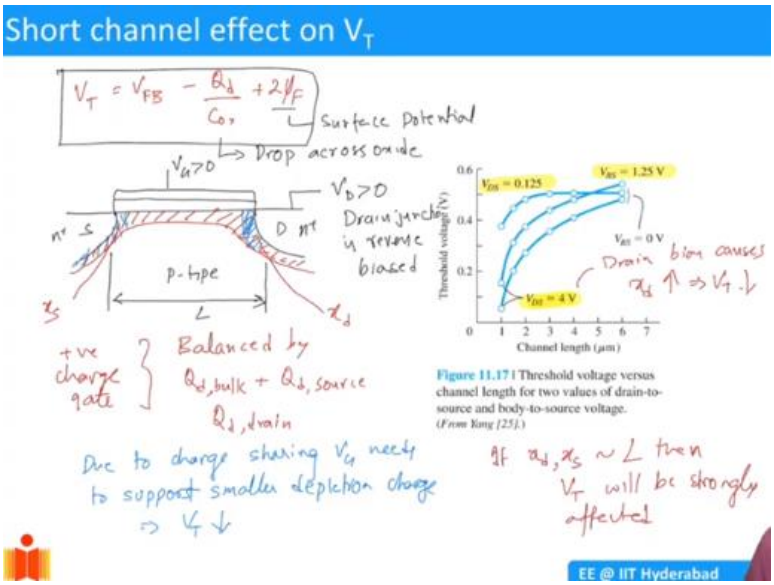

So if you look at the derivation for V_T that we have done you might recall that V_T had few components.

$$V_T = V_{FB} - \frac{Q_d}{C_{ox}} + 2\Phi_F$$

Now we did this for the case of a ideal MOSCAP and that exactly valid to the MOSFETs as well so you have the flat band voltage and then there is a –Q d by C ox term plus for the case of V_T you will have 2 psi F which is potential. So this part is a surface potential essentially the potential drop in this semi-conductor right. And this is my potential drop across the oxide.

And then of course flat band too account for the differences in the work function or the interface charges and so on. So this is a definition that V_T lay of studied so if you look at this expression do you think that there is any dependence of the channel length on the V_T. To analyze that what we will need to do is let us just look at the structure of a MOSFET so you have the source and the drain source drain. And then there is an oxide and there is a gate so if you look at it from the top to gate to the sub state that is simply a MOS cap.

And there are going to be this is P channel let us say P type substrate n channel device so this is N + and this is N +. Say in such a scenario you will have depletion region under the gate let us the V G is positive here V G is greater than 0. So there is going to be this depletion region under the gate and also the some depletion region around the source and the drain junctions because those are also PN junctions.

Now you should think about it if you just look at it only from the top to bottom should there be any effect of the channel length on the V_T well no right. Because we are not really considering you know when we derive this expression on the top we did not consider that type of channel on the top we did not even introduce channel at that point of time region. Simply to the MOS capacitor so how does the channel influence the V_T? To understand that we need to look at what is the channel length here?

The channel length is initially distance between the source and the drain is not it? Say now what is V_T? V_T is essentially gate voltage required to first deplete the substrate and then create inversion charges. So it has to support the depletion charge which is appearing the V_T expression as this $2\Phi_F$. So now when you have a long channel device and you must remember that there are this part of the junction which is supported by the source this depletion region is supported near the edges right.

This is supported by the source and the drain there also reverse biased correct. At best you know in this case of source at ground and bulk is at ground they should be some built in depletion width is something right. And then in the case of a drain junction in a typical NMOS right have actually V D greater than 0. So this drain junction is reverse biased right ? so what is happening is , The gate is supposed to support the entire depletion charge always you know in MOS capacitor device you have a positive charge and the gate say so the negative charges has to come from the substrate.

So now what happens is? You have 3 contributions so positive charge on gate right in the MOSCAP case it has to be entirely in the substrate region so depletion charge plus inversion charge that is what we say. So this is on one side of the equation this should be balanced by what? So you have the depletion charge Q_d is the bulk and then there is depletion charge in the source in the drain junctions.

So $Q_{d,\,source}$ I should write plus here because all of should be added up plus $Q_{d,drain}$. So at the drain junction and at the source junction also there is some charge which is been supported by the potential and the source and the drain not the gate. So this entire positive charge and the gate should be balanced by these 3 charges. Let us assume that inversion is not sourcing right now so this charge you know gate this balancing charge negative charge as to be shared by these 3 terminals of a drain and the source.

So because of that the amount of gate voltage necessary to create inversion is reduced because part of the depletion charge is supported by the source and the drain. So because of the charge sharing due to charge sharing V_G needs to support smaller depletion charge and this implies that V_T is reduced. Now well if your channel is very long then the amount of depletion charge at the source and the drain junctions is going to be very small insignificant.

But as you go to smaller and smaller dimensions now if you say that this is you know let us call it X_d the junction depth here the junction X_S. So if X_d and X_s you know let us say if X_d, X_s are comparable to L then V_T will be strongly affected. And that is what we see here I mean in the graph here we are showing different V_T for different channels length X axis the channel length. As you reduce the channel length what happens? So y axis is a V_T so let us take the case first of you know drain bias very small 0.125 125 milli volts.

So let us assume that it is in the linear regime so what happens? Well initially when the channel length is long nothing but happens if you reduce it. But once you fit the short channel regime when you are depletion width at the source in the drain junction is comparable to the channel length then the V_T starts reducing and this is a trend you see as you go to smaller and smaller channel length the V_T is reducing.

Because the gate is supporting lesser amount of depletion charge so the V_T is reduced now what happens is I apply a positive drain voltage you know the second case is here you have a positive drain voltage of let us say of 4 volts. So we know that this let me it should be , so drain bias causes depletion width at the drain junction. Let us say it is X_d we call it right causes X_d to increase that means VT has to even lower.

So that is why we see that it reply V_T lower right that is how when you compare with no drain bias which is first situation small drain bias which is only 1 to 5 and compare that to reasonable large drain bias of 4 volts. If you introduce that essentially your depletion width on the drain side is going to much larger and so, that impact is going to be strongly shifted. So this is how the V_T will faster and what if you applied a bulk potential.

In this bulk is P type right and I am applying a VBS of 1.2 volts and positively biasing so forward biasing drain bulk junction. If I forward bias is at drain bulk junction I reduce my depletion width. So the gate has to you know we have to apply greater voltage at the gate to support the gate amount of depletion charge that is why you expect that you know the V_T is higher initially in the case of the positive bulk.

But then if you go to smaller and smaller channel lenghts we are actually making it easier the barrio is lower than the source side. So you are actually making easier for the current flow that is why V_T falls but still it is going to be compared to VBS of 0 it is going to be higher. So these are

the trends so when you look at it for the first time I am sure it can be slightly confusing. So my effort here is not really to make sure that to understand all the details.

I want you to understand what are the factors that you need to consider? So my strong suggestion is to stop the video here just look at the graph and try to explain in your own words that will clarify your thoughts. If you feel that somewhere here actually missing the link then you go back and revisit the video and then again do it one more time. So that you should not write remember this and there is no way that you will remember you will forget it eventually.

So the better approach would be try to analyze it for yourself and see it what comes out okay. So based on the principles we have developed in the MOSFET's and even the PN junction. I think explanation that should come forward so whatever I have discussed just you know will be here helpful for you to analyze for yourself. If you still have any question of course you know I am available for a discussion so we can do that.

I am just trying to tell you that as you go to more advanced technologies this becomes more complicated. It is not the simple things that we learn so we need to aware of these things now a days nobody really you know we have a lot of computer to be help us calculate all these things. So we do not do it with pen and paper any more all of this design using computer aided tools TCAD tools we call them. Technically Computer Aided Design we call them technology computer aided design.

So anyway so I just wanted to introduce to what are the various factors that are made alright. This is the short channel effect now there is one more thing that we can do.

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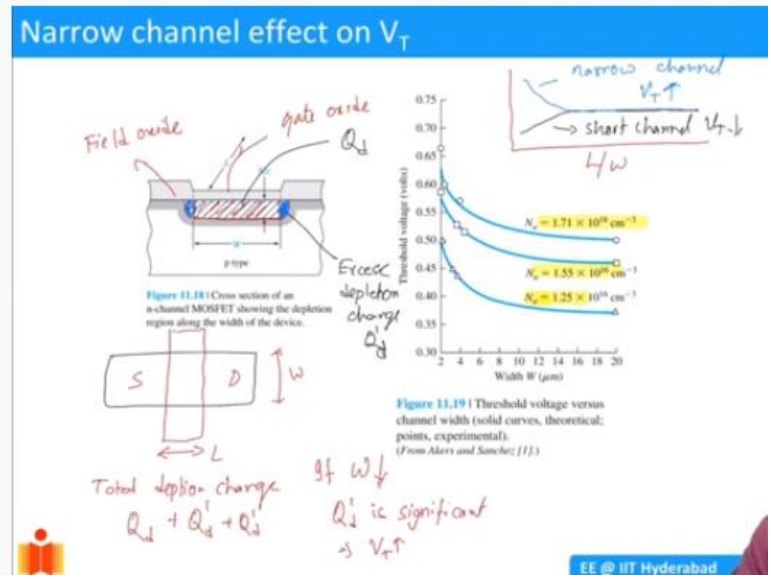

Which is Nano channel because you know when you remember we talk about MOSFET the top view of the MOSFET right we discussed it couple of times wherein we had this source and drain region and we said this is the gate on the top if you look at it. So this is my source this is my drain this is my length of the channel right. So length of channel is what plays a lot of you know important roles we discussed related length. So you always kept drawing the band diagram along the source to the drain.

But then another important feature is the width if you increase the width of the transistor then more current flows right. But then if you are scaling or scaling down the width as well right both length and width have been scaled. So what, happen it will go to smaller and smaller width so here the V_T behaves like exactly opposite to the narrow short channel. If you make a narrow channel, that is, you make it less wide the V_T increases rather than decrease in the previous case.

Why does that happen? Well to understand that you need to visualize the MOSFET a little bit so I have shown some 3 dimensional pictures as well in the beginning of MOSFET discussions as you can go back and look at it. So what happens is? You take the cross section along the width and this is how it looks so you have the gate oxide here this is gate oxide and under gate oxide there should

be depletion region. If you apply a positive voltage right on to the gate then it should deplete this is my depletion region under the gate oxide.

But it is never going to happen that will be exactly under there is going to be some penetration on the depletion region under the field oxide. So this region right which is supposed to be field oxide right means it is meant to isolate 2 different transistors so that they do not talk to each other. So but when you apply a gate voltage some of the gate voltage or you know gate charge is going to be spent in balancing some depletion charge under the field oxide it is going to be some spread under that.

Because you are never going to be perfectly vertical lines well if you are width of your device is large. Then this is not really a matter let me call I think here your let me call it as excess depletion charge Q_d depletion charge. This is excess depletion charge so when your channel is wide the fraction let me call it Q'_d the Q_d is basically depletion charge under the oxide. So what is the total amount of charge that you have?

You should have total Q_d or you know total depletion charge is going to be Q_d which is under the gate $+Q'_d$ under you know one side of transistor and another side of the transistor another Q'_d .

$$Total\ depletion\ charge = Q_d + Q'_d + Q'_d$$

So this additional regions right this excess region that I called and putting it to inclusive dark blue. So this is a additional Q_d that you have to support under the field oxide. So if you have width is large then this Q'_d is going to be very small insignificant so it does not matter much.

But once you come to narrow channel devices in your width when it uses you have this additional baggage that you have to support additional depletion that has to be supported. So if we W reduce Q_d' is significant and it you have to support as well. So Q_d' is significant implies gate have to larger voltage so that you know you put a gate charge and balance out additional Q_d'. So V_T should increase and this is exactly what you see here in the picture and this is again taken from the text book.

If you look at the text book they will do lot of derivations and then you know try to convince you that but I would suggest you we do not require to go into all the derivations here. You just need to understand the physical affects that is enough for us. So this is channel width and this is the voltage so as you go to smaller and smaller widths you see that the threshold voltage is increasing. And of course because there is an additional data point here which is substrate doping.

If you increase your substrate doping then V_T increases this also I think I will leave it for you to analyze it should happen. We have discussed with some I know in depth when you talking about the MOSCAP C-V. So anyway this is the trend that is significant so to summarize there are 2 affects one is you know on V_T, one is let us call this you know length or width both are plot on the same graph.

So if you are length or width is large length is large I will put it in black if the length is large it is constant but once you come to narrow short channel V_T reduces. But you have a narrow channel initial the width was large V_T is not changing much. But then if you come to narrow channel V_T increases so these are the 2 prominent effects are happen. So this is again to tell you that the device design is complicated I mean it is not that simple.

But our fundamental that we learnt in the beginning part of the course right P N junction are in the MOSFET MOS CAP will help you understand all this things. So these are 2 effects of short

channels on short narrow channel on the V_T there is one last thing that we want to discuss briefly before I stop the discussion.

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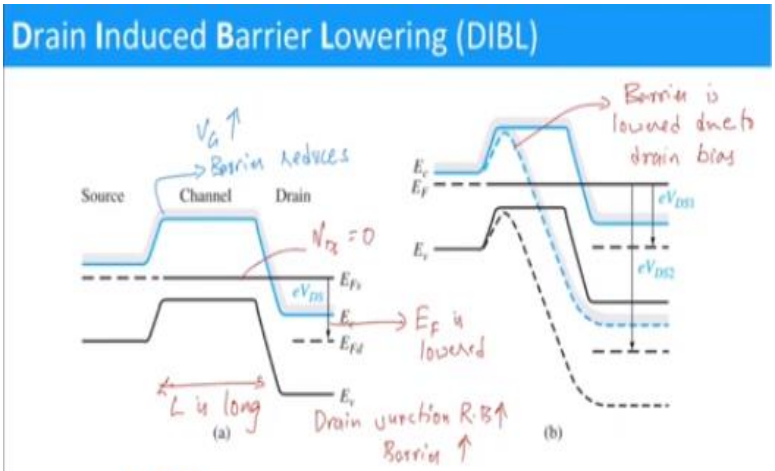

Fig 11.25 | Energy band diagrams of long and short channel MOSFETs showing the effect of drain bias

That is what is called as drain induced barrier lowering so we saw the band diagram when there is no drain bias applied. So we have drawn band diagrams on the source to through the channel into the drain. When there is no bias applied we saw that there is a barrier created and when you apply a gate voltage if I apply V_G here V_G increases this barrier reduces so current flows this is the basic operation of a MOSFET that is why the current flows.

Above a certain threshold the barrier is completely removed you have exponential large connect that is how we get it is like a P N junction you know when the barriers is reduced you have exponential using in current. So one question to ask is? There is drain voltage have an influence on the barrier initially if the channel length is long of if this channel length L is long right channel length is long what will happen if I apply drain voltage?

Let us say I am applying drain voltage is positive right for NMOS devices so what am I doing so this was the Fermi level of an equilibrium you know without drain bias right. Drain bias or I will call it V_{DS} equal to 0 but now I am adding a drain voltage I am increasing the drain bias and if I do that I am going to pull my Fermi level lower. Relative to the equilibrium case this you know this V_{DS} you know this is causing Fermi level to come down right E_F is lowered.

We have discussed this as that right when we are drawing the band diagrams but you know this is essentially a reverse bias. If you are increasing a V_{DS} your drain junction reverse bias increases that means the barrier height increases. But it does not really influence your current much because current is dependent on 2 barriers one is the source barrier one is drain barrier. The drain barrier is increasing but that should not affect your source barrier.

So you still have you know the similar current but the moment you go to short channel devices what happens well this is basically the picture of the long channel case. In a super pose on that it is short channel device if you have a channel device what happens is because you have to lower the Fermi level the drain side. Automatically the barrier is going to become smaller because this barrier is lowered due to drain bias.

Remember these barriers are energies right you do not have some quadratic relations things like that. It will not be the perfect junctions right it is going to have certain field depending on a charge density in a background discharge how it is depending on that you can calculate these things it is going to be some part of quadratic behavior but then you are forcing this because you do not have sufficient to voltage sufficient distance for it to flattened out.

So you are actually forcing the barrier to take a shape like this so what does it mean? We are actually making it easier for the charges to flow across the channel. This source barrier is reduced so the current should increase or VT should reduce correct so this is called drain induced barrier

lowering when there is nothing significant complicated about it. It is simply you know you should understand the basic band diagram you will see this immediately.

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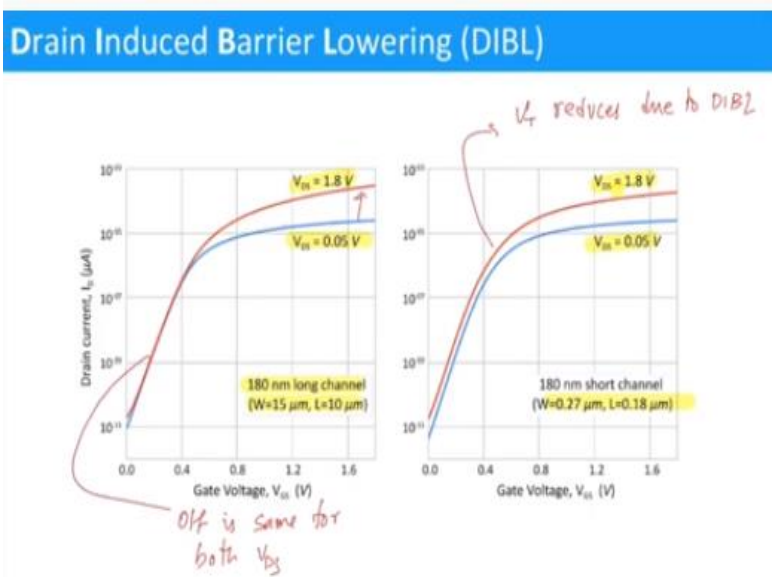

So how does that influence so this is the last thing that I want to talk about short channel effect. If you have a long channel device 10 micron long and you measure the I_D-V_G at 2 different drain bias of 50 millivolts drain bias of 1.8 volts. Basically change the drain bias and we discussed of course you know when you turn on the MOSFET is going to be a stronger current that is okay that is what you see here. So increase in the current is expected.

But in the off state when you have this barriers we do not expect the drain barrier to influence the current. Because of which you see that off current here is same are both V_{DS} this is what you expect in long channel device. But the moment you go to short channel device which is 0.18 micron length what should happen? Well you have the lower V_{DS} I_D-V_G and then if you go to higher V_{DS} because of the drain bias the barrier is lowered and because of which the V_T is shifted.

V_T reduces due to drain induced or I will call it DIBL straight away drain induce barrier level. So this is another feature that is notice in short channel devices so as I have told you before as well my goal is to simply outline few short channel affects that you need to aware of if you are pursuing deeper into the electronic study of electronic devices. This is not exhaustive there are many more things.

But of course this you do it a master level you do not need to do it at this point of time you learn it at a greater detail. So that you know you can understand the current technology there are many thing suppose this sort of features are very useful when you are trying to understand VLSI design. Because if you look at VLSI design there are computer aided tools CAD tools that will allow you to simulate various devices.

For most of the engineers is see that you know design engineer this is all blackbox simply do not understand what it is? But if you understand these basics then all of these SPICE models and things like that lot of sense. So you can actually look into the SPICE model and understanding what is happening and things like that. So it will give you a strong foundation for any VLSI design that you take in a future alright.

So that is it I would like to stop the discussion here so this lecture essentially we focused in a short channel effect. This is what happens if we have in a first video we have seen the current you know how the current changes for short channel device. And a second part second video we have seen the how the threshold voltage changes. So these things are very intuitive I mean you would not expect you to know it if you could not heard about it before.

But once you have seen the lecture I think it should be so it should sound intuitively correct that is my goal. So I will give you a few assignment questions we should help you to reinforce this concepts. Please try to attempt them and then if you have any questions we can discuss got it, So,

with that I will like to stop this lecture I will see you in the next lecture thank you so much have a great day bye.