Introduction to Semiconductor Devices
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Lecture - 62
CMOS Technology

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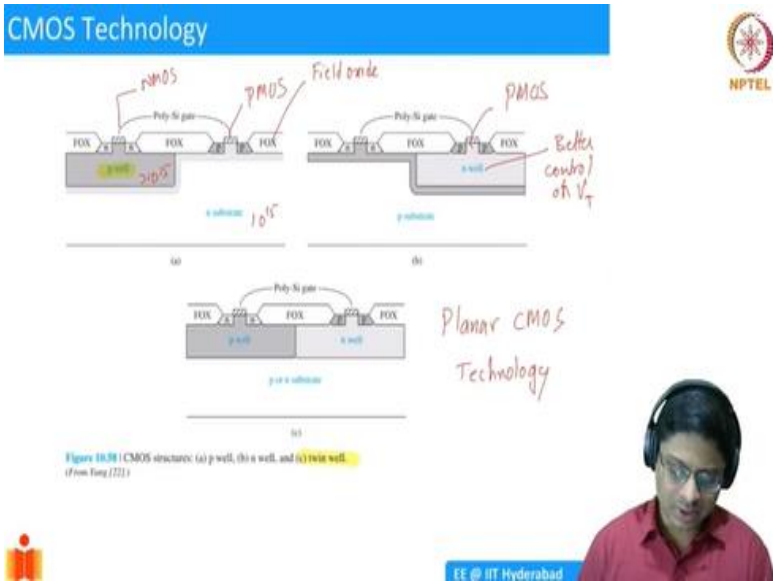

Hello, everyone, welcome back. So, we have understood various device related aspects of MOSFETs. So, I wanted to give a quick overview of how these are fabricated just so that you get an idea. So, the fabrication of MOSFETs is a very, very complicated business and to understand it fully you require a fully regulated course which will go into great depth. But our objective in this course is not to do that.

But we will just give you an insight into how it is done. So, we have seen that we have these NMOS devices and PMOS devices and we want to fabricate them on a chip and we have previously talked about what a nano fab is and we have seen some videos on that. I asked you to see some videos. So, you want both and most NMOS and PMOS devices on the same chip.

There are a couple of ways of doing that. For example, you could start with an n type substrate that is n type wafer and then when you have n type wafer you can quickly have p type diffusions. So, when you have source and drain p type regions you can make a PMOS device very efficiently. But then how do you make an NMOS device on an n type substrate?

To do that, we have to create a separate region which we call as a well region. Wherein, let us suppose the substrate doping is $10^{\wedge 15}$ and if we create a well with $10^{\wedge 16}$ doping of acceptors, then in this case, we will have a p type well. So, that is what is schematically shown here. So, we are taking a substrate which is n type. And then once I have that I can quickly make so strange diffusions of P. This is a PMOS device.

But to make an n type device, we have to create what is known as a p well. Because this was let us say $10^{\wedge 15}$ then I have my p well doping has to be at least in part you know greater than $10^{\wedge 15}$ it could be maybe $10^{\wedge 16}$. If I have that doping then I will essentially compensate the donors and then I will create more acceptors.

So, you saw that there is a compensatory doping and the substrate behaves like a p type substrate. And then you have these well regions which are source drain regions for your NMOS device. So, you can fabricate this. So, you can have different regions on a wafer which we can fabricate these devices. But then one important characteristic is that we do not want these devices to talk to each other.

Because this is ultimately a conducting substrate, there is going to be a lot of crosstalk so to prevent that you have to isolate devices from one another. So, this we do that using field oxide. This is no longer used, because there are some problems with it. Nowadays we use what is called as shallow trench isolation.

But that is not that we will be discussing in fabulous a technology course. But right now, this is a field oxide, which is essentially used as a thick oxide, we saw gate oxide, which is very high-quality thin oxide. But then you can also have a thick oxide, which we call us field oxide. That is

essentially isolating, you are creating barriers between different MOSFET devices. By the way, this is only one axis right there showing a cross section.

But in principle, this field oxide will be surrounding the MOSFET all directions, it is like a ring you are forming around a MOSFET to isolate it from other MOSFETs. So, that field oxide will be created. And you can then connect these devices to form various configurations. This iso one approach. But if you do this, you do not really have much control in the threshold voltage of the PMOS because whatever is a substrate, you are going to have that.

Whereas for NMOS device I am implanting the p well .I can control how much doping I am introducing into that so I can design my NMOS better with this. You could also take the other approach wherein I start with a p type substrate. So, I can have an NMOS like this like n + n + regions I can create and then I will create my PMOS device in n well .

So, whenever you have a PMOS device, you have to have a n well. So, we create an n well so you can have PMOS and NMOS devices on the same chip. But now if you do this, you have better control on the V_T. The well creates a better control on V_T. You are not dependent on the substrate doping but you can tune ,you can increase the doping density of the well in some locations and then increase your V_T.

So, eventually now, in the recent technologies what we do is? We have both n well and p well. This is known as twin well process. So, we take substrate any substrate it does not really matter p or n and then create a n well for the PMOS device and p well for NMOS device. And then you make this connection. So, this is a twin well process which is routinely used. Here we are only showing two transistors but I can repeat it billions of times to get billions of transistors on the same chip.

So, that is how this this entire process is known as planar technology or planar CMOS technology. This is the most dominant form which was up to about 2011 or so, just 9 years 10 years back till then we were using this even in the most sophisticated chips. This is what was used. But then in

the last 10 years something has changed and we will talk about it towards the end of the next week. So, this is CMOS technology.

And this has been the workhorse of semiconductors for about what 40 years easily. Starting from 80s when it became dominant to about 2010 around three decades. So, what how does it help us?

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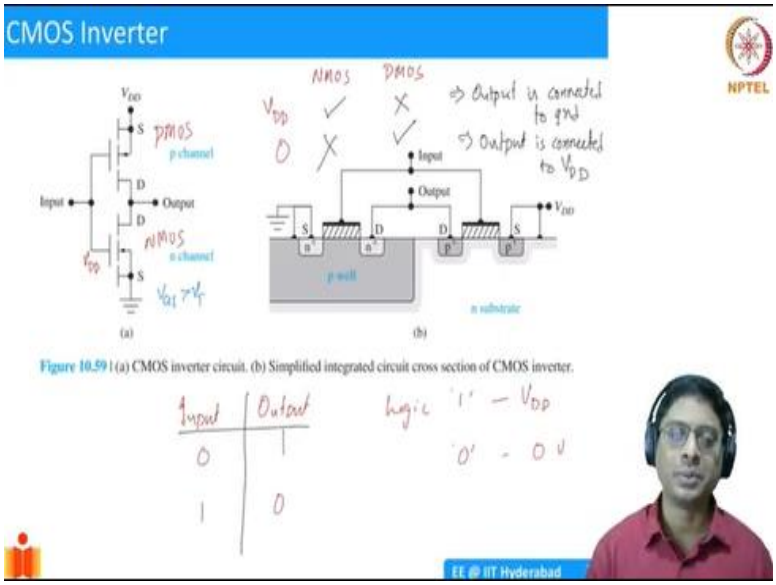

This is the simplest form of a CMOS device that you can think of, wherein I will connect NMOS device and a PMOS device. This is a different representation for a MOS, this is basically meaning that this is PMOS and this is NMOS.

So here both gates of NMOS and PMOS device are connected together we call it input. And then the drain of both devices are connected called as output. The source of NMOS device is connected to ground and the source of PMOS device is connected to V_{DD}.

Just two transistors which are connected and physically if you look at it will be something like this, you have the p well which is having the NMOS device. And entire substrate so, you have PMOS device here. So, the drains are connected like this and then the source is grounded, this is V_{DD} and how is this exactly done? How these connections are made? Well, it is something similar to what you see on a PCB when you see a PCB you see this component.

And there are these copper lines which are running. So, those are all metal connections that we are making. Something similar happens once you make the basic device you will do what is known as metal layers on the top of the wafer. And then this this can be many many metal layers and then lots of connections are made imagine you know, if you even ever try to design a PCB with let us say 100 components you did understand how difficult it is to do the layout.

But now we are talking about networks connecting let us say billions of transistors. So, you are going to have a lot of complications. So, there is a lot of planning that is involved in actually how to do the layout. But, it can be done. Once you have this inverter what happens? So, inverter, is basically a logic gate wherein I have my input and output let us say, when I input is 0 output should be 1 when my input is 1 output should be 0.

How does this happen? What does voltage physically mean? Logic 1 means V_{DD} supply voltage, logic 0 means 0 volts. This is electrically correct. We are just using that we are referring it as 1 and 0. That is a Boolean representation of the voltages. Physically it has to be some voltage. So, let us apply one that means I apply V_{DD} here. If I apply V_{DD} to the input, what happens to this guy?

When this is V_{DD}, V_{GS} is definitely greater than V_T. So, now, in this case, V_{GS} is greater than V_T. So, NMOS is on. So, when my input is V_{DD} input is NMOS device is going to be on because V_{GS} is greater than V_T. What is the V_{GS} of PMOS device? Zero. And it needs to be negative V_T, - 0.5 let us say.

So, it has to be smaller than that. It has not been the -1 or something when V_{GS} is -1 then the PMOS device will conduct. So, this will be off. So, what does it imply? This implies that output is connected to ground. So, because this is on; output is really connected to ground. Now what happens when your input is 0? When your input is 0 what is V_{GS} of NMOS device? V_{GS} of NMOS device is 0, it is less than V_T.

So, in this case my NMOS device is going to be off whereas, PMOS device input is 0. So, V_{GS} is - V_{DD} which is less than the -V_T of the PMOS(negative sense). So, PMOS devices on. This implies output is connected to V_{DD}. Output connected to V_{DD} means output is 1 output connected to ground

means, output is 0. So, that is how you get this logic, 0 and 1. This is the simplest CMOS circuit that you can think of.

And the beauty of this circuit is at any point of time except during the switching if I am at 0 or at 1. There is no direct connection from the V_{DD} to the ground. So, current cannot flow. And we already saw that, input is actually having very high input resistance, there is no current due to this. And this path also, only one of the transistors is on at any point of time, not both. If both are on, it is going to continuously dissipate power.

If one of them is off, let us say this is only having 100 picoamps of current. This even if it is one milliamp current, I do not care. Now once the output discharges you do not have any current flowing to this as such. So, the overall current will be very small amount. And so, we have a very power efficient circuit. And that is the reason why CMOS has become the most dominant technology.

Because in static case when, let us say inputs are 0s or 1s, not during switching. Switching, there is going to be some power dissipation, but only when it is 0 or 1 at that static phase. There is no power very, very negligible power dissipation. It is not like that in BJT's. If you have a BJT you try to make an inverter you could make an inverter like circuit, but then it will continuously flow current.

And because of that the power dissipation will be so much that you are let us say you made a transistor out of BJT. I do not think it will last even five minutes. It will depend upon the battery of course. But it is not at all a very efficient device it will just heat up like crazy. So that is why CMOS is very popular. And so, this was just a quick overview of what CMOS can do.

We can design you know what is the CMOS logic, NAND gate NOR gates and so on. There is another course on CMOS design that can also be taken wherein you understand how to make NAND gates NOR gates, what are the trade-offs? How do you choose the width to length ratio of these structures? How do you design them? All that is an additional course on CMOS VLSI design from the transistor perspective.

So, of course, we will not cover that in this course but that is something that you will learn later stage. So, thank you so much for your attention. And I will stop here. I will see you next week. Have a great day, bye.