

Introduction to Semiconductor Devices
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Lecture – 60
Example Problems with MOSFETs




This document is intended to accompany the lecture videos of the course “Introduction to Semiconductor Devices” offered by Dr. Naresh Emani on the NPTEL platform. It has been our effort to remove ambiguities and make the document readable. However, there may be some inadvertent errors. The reader is advised to refer to the original lecture video if he/she needs any clarification.

Let us get back to the discussion of MOSFET. So, in the previous video we derived an expression for the current in a MOSFET. Let us try to get a typical number for a MOSFET.

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Long channel MOSFET – example problem

The parameters of an n-channel silicon MOSFET are $\mu_n = 650 \frac{\text{cm}^2}{\text{V}\cdot\text{sec}}$, $t_{ox} = 8 \text{ nm}$, $\frac{W}{L} = 12$, $V_T = 0.4 \text{ V}$. If the transistor is biased in the saturation region, find the drain current for $V_{GS} = 1.2 \text{ V}$

$$I_D = \frac{\mu C_{ox} W}{2L} (V_{GS} - V_T)^2$$
$$= \frac{650 \times 440 \times 10^{-9} \times 12 (1.2 - 0.4)^2}{2}$$
$$= 650 \times 440 \times 6 \times 0.8^2 \times 10^{-9}$$
$$\sim 100's \text{ nA} - \mu\text{A}$$
$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}}{8 \times 10^{-7} \text{ cm}}$$
$$\sim 4.4 \times 10^{-7} \text{ F/cm}^2$$
$$\sim 440 \text{ nF/cm}^2$$


By doing that, I want to introduce what is known as a long channel MOSFET. When I say long channel typically, I would say that the channel length is more than one micron. These are the traditional newer devices which are used in the 80s and early 90s. But after that the technology has developed so much that the channel length became less than one micron. And when that happens, there are a lot of other short channel effects that come into picture that we will be discussing in the next week.

Like when I say long channel, take the approximate channel length to be one micron so that we do not have to worry. If you get to a small channel then there are a lot of other effects. This is

a problem, I believe it I have taken it from the textbook .So, the parameters of an n channel MOSFET are given us in a mobility which is 650 centimetre square per volt second.

C_{ox} is given to you, W by L is given to you, V_T given to you, if the transistor is biased in saturation regime what is the drain current for $V_{GS} = 1.2$ volts. So, I mean well this is a straightforward problem, but I just chose it to highlight a few points. One is, what is the mobility that we remember from the early discussions in the first couple of weeks? The mobility of NMOS was I think 1350 centimetre square per volt second.

Whereas the mobility now given is 650 centimetres per volt second. Why is that happening? Well, it turns out that we have an interface phenomenon, the mobility in the bulk is still 1350 centimetres square per volt second. That is the most commonly agreed value, but when we come to the surface you know, we are dealing with an interface between silicon and silicon dioxide.

So, whenever you have such an interface there will be scattering with no interface traps. There are few numbers; silicon dioxide interface is very good. But even then, we have some scattering and because of that there is some degradation of the mobility. That's why the mobility will be smaller, interface mobility will be smaller, surface mobility will be smaller than the bulk mobility. That is one point that you know, it is going to come back.

We are going to tell you how it influences the drain current and all that later. So, let us try to solve this problem. So, what is the drain current? Well, it is in the saturation regime, the drain current equation is given as,

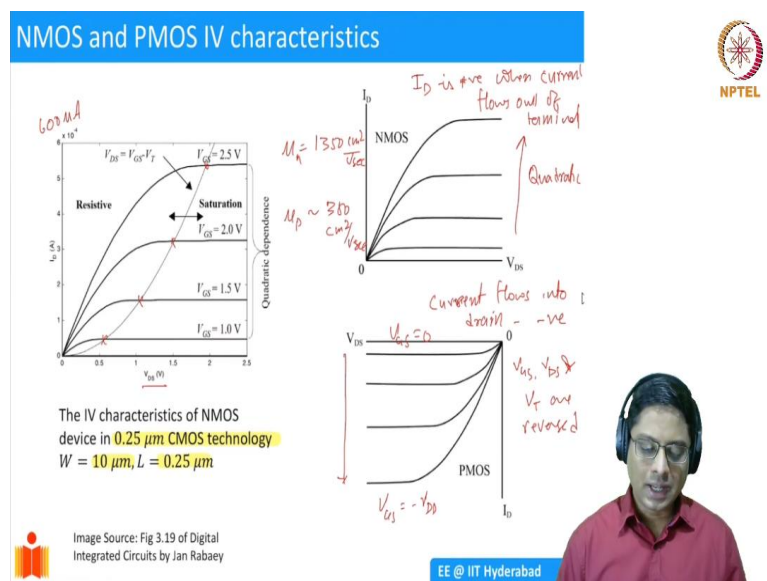
$$I_d = \frac{\mu_n C_{ox} W}{2L} [V_{GS} - V_T]^2$$

So, this will be simply plug and chug 650 centimetres per volt second multiplied by C_{ox} , what is the C_{ox} ? Well, that could be you know, we did it for the MOS caps. This will be epsilon oxide divided with thickness of oxide this will be $(3.9 * 8.85 * 10^{-14})$ divided by C_{ox} which is 8 nanometres, which is $8 * 10^{-7}$ centimetres. So, I can calculate this well, 3.9 is approximately equal to 4, so 4 by 8 so 2.

So, C_{ox} will be approximately equal to 4.4×10^{-7} farad per centimetre square. Now, I_D should be 650×440 nano farads per centimetre square, W by L is 12. This is divided by 2 into V_{GS} is $(1.2 - 0.4)^2$. This is the limit of what I can calculate approximately. So, $650 \times 440 \times 6 \times 0.8^2$, there is a big 10^{-9} .

Well, when you calculate it will be something in the range of, let us say 100s of microamps to milliamps, something in that range. We will just substitute and check this. So, this is a typical number for a MOSFET.

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And I told you that I will show you the exact drain current calculated for CMOS technology, this is basically what we refer to as 0.25 micron CMOS technology. I will explain that when I discuss scaling more, and the device width was 10 microns, the length was 0.25 microns. And if you have such a device, you see that as your gate voltage is changing, this is V_{DS} versus I_D as the gate voltage is increasing, the drain current is increasing quadratically.

And the drain current is going from 0 to 600 microns, you see that there is a reasonable amount of change in the current. So, whenever you turn on the MOSFET you have large current. When V_G is less than V_T , then it is zero current. So, that is how MOSFET acts like a switch. Simultaneously you also see that at particular V_G sat or V_D sat, for each gate voltage you have a quadratic increase in the drain current.

So, this is for a NMOS device. So, far we never really discussed much about the PMOS device, but it turns out that the PMOS characteristics are also complimentary. The only difference is that the mobility of PMOS devices is much smaller. So, the current will be smaller in the PMOS devices. Because remember that μ_n for NMOS was something like 1350 centimetre square per volt second where μ_p was, I think it was 400 or 350 centimetre square per volt second.

So, this is a bulk mobility, when you come to surface it will be even smaller. So, the PMOS currents will be smaller. So, how do we deal with it, how do we increase the current in a PMOS device? Since mobility is smaller typically, we take the PMOS transistor to be wider with the W we take it to be larger to get the same currents. So, this we have already seen the quadratic variation in the current.

When you go to PMOS devices, we have exactly complementary situation. In NMOS device, the electrons are entering into the drain, because V_D is positive and electrons will enter into the drain. So, by convention we take the drain current I_D basically means is positive, when current flows out of the terminal. When you take a PMOS device you have holes which are moving and they flow into the drain.

So, here current flows into drain and that is why we take it to be negative, the convention for current is negative now. And also, V_{DS} , V_{GS} , V_T all of them will be negative. So, basically flip the signs of V_{GS} , V_{DS} and V_T . That is usually the typical well designed PMOS device which will be complementary to the NMOS device. That is why your drain current will be in this fashion, quadratically increases in the negative direction as V_{GS} increases.

Now this would be $V_G = 0$. This would be V_{GS} equal to $-V_{DD}$. So, as you go to minus voltages it increases. So, this is how the PMOS device behave, it is exactly complimentary. So far what we have seen is, the parameters of the current rate expression are fixed like, for example mobility, capacitance and all are dependent on the process, W by L is fixed by the designer when you are fabricating the chip you can fix it.

So, if you want to change the current, we have seen that V_{DS} can be changed and V_{GS} can be changed by the user. That is what we have so far. But it turns out that user has another way to change the current in a transistor and that is by using what is known as body effect.

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The slide, titled "The Body Effect", illustrates the physical mechanism and its quantitative impact on the threshold voltage of a MOSFET. It features a cross-sectional diagram of an n-channel MOSFET on p-silicon, with source and drain regions (n+) and a gate stack (Metal/Oxide). The gate voltage is V_G , source voltage is V_S , drain voltage is V_D , and body bias voltage is V_B . Handwritten notes explain that a negative V_B creates a reverse bias at the source-body junction, leading to a "Source-channel barrier" that increases the threshold voltage V_T . The equation for the threshold voltage is given as $V_T = V_{T0} + \gamma \left(\sqrt{2q\phi_F - V_{BS}} - \sqrt{2q\phi_F} \right)$, where γ is the body effect parameter. A graph plots V_T (y-axis, from 0.4V to 0.85V) against $-V_{BS}$ (x-axis, from 0 to -2.5V) for a 0.25 μm MOSFET, showing a linear increase in V_T with $-V_{BS}$. The NPTEL logo is in the top right, and "EE @ IIT Hyderabad" is in the bottom right.

So, when I introduced the MOSFET in the beginning I said that you have these four terminals and we said that the body is grounded for NMOS transistor. For a PMOS transistor, it is at the supply voltage V_{DD} . But it needs not be the case. We can actually change the voltage at the bulk or the body. This is V_B ; V_D is drain voltage, V_S is grounded typically and this is V_G . So, far we have seen that you know you can control this.

But you know V_B does not appear in our current expression. So, current expression is simply function of V_{GS} and V_{DS} as far as the user is concerned. Does V_B appear, well it actually does but indirectly. The reason is let us try to recollect how the current flows between the source and the drain. The current flows because I mean there is a barrier. Let me go back the energy band picture, let me say I have a constant fermi level.

And then I have n type source and n type drain. And then I have a p type channel. Because of that, I have a band which is forming like this, this is a band diagram. We showed it when we discussed the subthreshold. So, we said that the electrons experience a barrier at both the source junction and the drain junction. So, they cannot enter into the channel. But what happens when you increase V_G ?

Well, as V_G increases, the barrier is reduced and you can have currents which are flowing into the channel. That is how the current flows, we have seen the quantitative way of deriving the expression. But qualitatively we are essentially lowering the barrier in the channel by

increasing the gate voltage. We saw that as you give a positive voltage to the gate, the bands move down, that is why the barrier reduces.

Now, let us say I use my bulk voltage and actually apply a negative bias to the bulk. What happens if I reverse bias this junction. I will apply a negative voltage, that means I am essentially going to reverse bias source bulk junction. In S B junction, Source is n + and B is p, so that I will reverse bias, I will apply negative voltage. What will happen when you apply a reverse bias, the bands move up.

So, when you reverse bias, source - channel barrier becomes larger, source channel barrier increases. And if the barrier increases, gate has to work harder. So, V_T increases so that we get the same level of current flow. So, in a way by using my fourth terminal which is a bulk voltage if I apply a negative voltage for a NMOS transistor so that I reverse bias my source bulk junction, then I increase the barrier for the electrons.

And because of that the V_T has to be larger and this effect is known as body effect. So, if you look at the V_T versus $-V_{BS}$ plot, negative of V_{BS} I am plotting. So, as I increase more and more negative voltage into the bulk, it becomes that much harder for the gate to turn on, so V_T increases. So, you will have a curve which looks like this typically. It would not be exactly a straight line, but more or less.

So, for a 0.25 micron CMOS technology, this will be about 0.4 volts. And this might be something like, let us say - 2.5 V, I wanted to apply. It might become something like 0.85. So, I can effectively double my V_T , it is possible to do that. So, this effect is known as body effect, wherein I am changing the threshold voltage of the MOSFET by applying a voltage to the bulk.

And the way to calculate that would be, there is an expression for that I will not derive it or prove it, I will simply give an expression which is going to be like this.

$$V_t = V_{t_0} + \gamma [\sqrt{2 \Phi_F - V_{BS}} - \sqrt{2 \Phi_F}]$$

So, this particular term γ is known as body effect parameter. It has a unit of $1/\sqrt{v}$ that will be given to you by the technology company. So, what it tells you is that, you have the surface potential, which we know at the threshold, which is $2\phi_F$.

If you apply negative voltage, this first term is going to be larger than the second term. So, that is why the threshold voltage increases. So, this is a simple way of trying to capture that. I said it is not linear because V_{BS} is coming in the square root, but we do not really change it that much. So, we can calculate the threshold voltage at a particular body bias. You might ask what happens if I forward bias my source bulk junction?

Well, if you forward bias it, you are going to reduce the barrier and the transistor action will be lost. That is why we do not really forward bias the bulk source or bulk drain junctions, that should be avoided. So, that is why typically, in mosfets, we ground the bulk for a NMOS device. So that if I apply whatever positive voltage, I am going to reverse bias it. It will never go into the forward bias.

Similarly, for a PMOS device, I will tie it up to the supply voltage. So that if I apply any other voltage, it will not go into the forward bias, it will always remain in the reverse bias. So, this is how the transistor currents can be changed. So to summarize, the main tools that we have as a user is that we can change the drain voltage, gate voltage or the bulk voltage. All of them with respect to the source and we can calculate.

So, if you have a body effect, well the V_T changes. If body voltage was 0 then you have V_{T0} , which is the default V_T or it can change depending on the body effect. And in the next lecture, we will talk about some performance metrics like, what are the different ways of evaluating a MOSFET? And we will go over from that.

We will also discuss things like subthreshold slope and all that which are very, very important.