Introduction to Semiconductor Devices
Prof. Dr. Naresh Kumar Emani
Indian Institute of Technology, Hyderabad

Lecture – 59
IV Characteristics of a Long Channel MOSFET

This document is intended to accompany the lecture videos of the course "Introduction to Semiconductor Devices" offered by Dr. Naresh Emani on the NPTEL platform. It has been our effort to remove ambiguities and make the document readable. However, there may be some inadvertent errors. The reader is advised to refer to the original lecture video if he/she needs any clarification.

Hello everyone, welcome back. So, in the previous video we understood how MOSFET operates. So, qualitatively we have explained what is meant by sub threshold? What is meant by linear and saturation regimes? So, today our goal is to get a more quantitative understanding.

(Refer Slide Time: 00:34)

To do that, we will start with deriving an expression for the current in a MOSFET in the linear regime. Remember when we said linear regime VDS was small, VDS~50 to 100 millivolts. So, how do we derive an expression for current? To understand that we need to notice a few things that is you know this is a schematic of a MOSFET. You see that there are the source and the drain regions.

And when VG is greater than VT you have the inversion layer which is found here just below the oxide. And of course, the MOSFET is a three-dimensional device. So, along with the length, which is the distance between the source and the drain here this is the length. You also have a second dimension which is going into the paper here into the slide. Where that is the width of the MOSFET we introduced that as well in the last lecture.

So, now, if you want to derive the expression for current, what do we do? Well, we need to understand what is a charge density first, current is simply charge density divided by time. So, what is the charge density? To get to that, we will start with the definition of VT,

$$V_t = \phi_{ms} - \frac{Q_i}{C_{ox}} - \frac{Q_d}{C_{ox}} + 2\phi_F$$

So, this particular first two terms we call it as V FB flat band voltage. Essentially whenever you have nonidealities applied flat band voltage should be nonzero. And $2\phi_f$ is a surface potential which tells you how much is a potential drop across semiconductor and this is the oxide voltage drop. So, that threshold, at threshold voltage you have this relation that is satisfied. Now, if you increase VG about threshold what happens?

We said that there is a quick build-up of inversion charge below the oxide and it behaves like a parallel plate capacitor. So, we can write an expression for VG just above the threshold.

$$V_g = V_{fb} - \frac{Q_d + Q_{inv}}{C_{ox}} + 2\phi_F$$

So, there is an initial inversion charge right below the oxide.

Surface production does not change, surface potential reaches the maximum value of $2\phi_F$ and it stays there. That is a delta depletion approximation. In reality then a small change which is negligible anyway for our purposes. So, this I can again, you know, simplify as simply:

$$V_g = V_t - Q_{inv} \backslash C_{ox}$$

So, now expressions for Q inversion.

$$Q_{inv} = -C_{ox}(V_G - V_t)$$

So, compare it with a parallel plate capacitor. So, in a parallel plate capacitor, we know that Q=CV. So, if you apply voltage V, we will get a charge Q, capacitance is Cox.

Similarly, here VG – VT is essentially the excess gate voltage or basically gate voltage over VT. If I apply that essentially, I am going to get a charge inversion charge which is proportional to the capacitance Cox times the excess gate voltage. So, that is a very nice and elegant expression. But remember this charge is basically for expert sorry not charge Cox here is $\frac{F}{cm^2}$.

So, your charge is going to be $\frac{C}{cm^2}$. So, if your VG increases Q inversion is going increase this proportionately. So, this is a very nice expression for us to calculate the total emission charge density. So, now what is ID? Inversion charge which is if your VDS is low, it is more or less uniformly distributed.

And the density does not change which position. But now, so the current will be ID will be simply the charge total charge divided by the time it takes for it to move from let us say from source to the drain. So, I write the current as the charge density Q inversion, I will drop the negative sign because that can be taken care of and sign convention you do not, I do not want to explain that now.

Eventually you know for drain current in the convention is that the, current comes out of the drain because electrons move into the drain. So, current comes out so, that is taken as positive. So, we can write this as the charge density which is simply:

$$I_D = \frac{C_{ox}(V_G - V_T)WL}{\tau}$$

$$\tau = \frac{L}{velocity}$$

$$\tau = \frac{L}{\mu E}$$

$$\tau = \frac{L^2}{\mu V_{DS}}$$

$$I_D = \frac{\mu C_{ox} W(V_{GS} - V_T)}{L} V_{DS}; \quad When\ V_{DS} is\ small$$

You will see in a moment that this will not hold true when V DS is large. Is it dimensionally, correct? Let us check it out. What should be mu? μ is mobility which is simply $\frac{cm^2}{Vsec}$.

Cox is Farad per centimetre square Wand R length units. So, they will cancel out. And then this is voltage square voltage VGS – VT is voltage and VDS is voltage, voltage squared is Coulomb per second. So, well this is correct. So, dimensionally we have satisfied. So, Coulomb per second which is current amperes.

So, what does this expression tell us? Current is directly related to the gate voltage and also the drain voltage. If you apply greater amount of drain voltage, you get larger amount of current, which is not surprising. And if you increase the gate voltage, you are increasing the amount of inversion charge which is present. So, you will have larger amount of current.

So, I can plot out another you know, I will define R linear.

$$R_{linear} = \frac{V_{DS}}{I_D} = \frac{1}{\frac{\mu C_{ox} W (V_{GS} - V_T)}{L}}$$

So, what does this tell us? It tells us that if you see the; you take a MOSFET in the linear regime that means you plot VDS vs ID you get current which is you know the relation is linear and you get a curve which looks like this. Let us call this as VGS1 at some gate voltage, that has to be above threshold remember below threshold it is going to be 0 flat. As we increase the gate voltage, it goes up.

Now if you take an even higher gate voltage, you are going to increase the amount of inversion charge because of the resistance drop. And so, if I take another VGS this will be VGS2 greater

than VGS1. So, the resistance drops, because of that at a particular VDS you have current increasing, so we as VGS increases, current increases. This is the linear regime of a MOSFET. So, we did not really do much in this we just understood what is the relation between the inversion charge.

And gate voltage and from that we derived the expression. But towards the end of the last lecture, I mentioned that if VDS is substantial we are entering the saturation region when there is something else that happens like.

(Refer Slide Time: 13:55)

So, what we said was the channel gets pinched off. While some of you might really not be very comfortable pinched off, even now, because it takes a little bit of time to appreciate it. So, what we are saying is, if you have a MOSFET, let us say you have the source and the drain, and then you have an oxide which is there on top. And now this is gate, let us say VG or apply. And let us take an example and say that this is equal to 1volt.

Now, when VDS was 50 millivolts. Essentially, you're the difference between source and drain is very small. And let us say I will apply VD = 1 volt is almost compatible to the gate voltage. Then what happens? What we said in the previous lecture was that as VD increases, it is essentially a piece of semiconductor. So, voltage has to drop across that. So, how will the voltage drop happen?

Let us say we know that this is anyway grounded. So, let us say at this edge my voltage was 0 let us say somewhere in between it is 0.25, somewhere else, it is 0.5, 0.75 and 1 volt when you come to this. So, essentially what we are saying is there is a variation of voltage across the channel and which we call it as Vx. So, this is basically Vx which is variation of voltage across a channel.

Now, if you want to create inversion charge. What is the voltage required on the gate? How much you know we already saw that the inverse in charge is essentially excess gate voltage, I mean gate voltage VT. If your gate voltage is below VT, you do not have inversion charge. Now, what is happening is? In the linear case, the variation across the channel was nothing, it is negligible. So, we took it as 0 and we took a uniform charge density.

But now there is a variation of voltage across the channel. So, we have to talk off what we can call as VGC, VGC means I am taking voltage at the gate -Vx. So, at each point on the channel, I have a different voltage because it is just behaving like a resistor. There is some amount of resistance it might be large might be small whatever, you have some resistance. And so, this VGC has to be greater than or equal to VT.

What happens if it is less than VGC? When there is no inversion charge at that location. And because of that, we have drawn this picture towards the end of the last lecture, we have shown you have this kind of a thing. We can say two scenarios, one is if I take this to be my drain and distribute my source and this red curve should be when VDS = VGS - VT, which I will call is really set the saturation drain voltage.

So, if you reach that point really is VGS - VT, what happens to VGC you can substitute and see that VGC will be quite exactly equal to VT, when you are at VDS equal to VDSAT then VGC will be exactly VT that is why you have almost negligible inversion charge. And if you go beyond that, for this black curve, this is basically VDS greater than VDSAT. If you do this the channel is getting pinched off you do not have sufficient voltage.

If you calculate VGC now VGC is less than VT so no inversion charge, near the drain end. But we still have substantial amount of charge already because near the source we have a charge and that

is what is being depicted by the sort of a variation. So, even in this is another picture from Streetman essentially showing you that as you approach the drain side there is a drop in the inversion charge density.

So, this can sometimes be misleading this does not mean that in space there is a distribution it is still inversion charge right under the interface, but the density is different. You could probably different depicted by colour graph, but this is this is what usually we do. It is simply telling you that density is varying not the physical distribution along the y direction it is still the same. So, now, when we have this sort of a variation of potential across the channel, how do we calculate the current.

And to do that, we employ what is known as a gradual channel approximation essentially saying that, the voltage across the channel is gradually changing. And in the picture below, we are showing that there is some sort of distribution. $x = 0$ here in this case would be the source and $x = l$ will be the drain. So, between source and drain there is a distribution of voltage and a first approximation can be linear but well the accurate one turns out to be this gradual, some sort of a quadratic relation.

So, now what happens you know what does the gradual channel approximation tell us? It simply tells us that there is a variation of inversion charge across the channel. So, now in the linear case it was uniform, density was the uniform everywhere. But now there is a variation in the density. So, Q inversion is actually a function of x and also this is kind of subtle but it assumes that the gate voltage in the normal direction.

That is from the gate to the oxide to the semiconductor that y direction in in this picture here y direction is basically depicted here and this is the x direction along the channel. So, what it tells you is that in the y direction whatever you have gate voltage that that field is much stronger than the field across the channel. Well, it is very reasonable approximation, what is the gate oxide thickness? Maybe; 10 nanometres, 5 nanometres.

So, the fields are going to be very large compared to channel lengths which are maybe 10s of nanometres. So, when you compare with the channel length it is definitely true that the vertical field across oxide is much stronger. So, this just makes sense it is important because you know we are kind of neglecting the horizontal field and if you actually have to do it accurately, we have to take both fields into account and then it becomes more complicated.

We have to do it numerically we cannot do it analytically easily. So, but anyway this seems to be a reasonable approximation, especially when channel length is long. So, we will discuss about what is long channel? What is short channel? come on down the line. But traditionally the channel lengths you know not my consequence of my 10-micron 5-micron 0.25-micron and so on. We will discuss more about that.

Also, we are assuming that there is no leakage from the oxide gate oxide. Well, that is an ideal silicon dioxide ideal insulator we are assuming that that is still holding true. If not, we will have some trouble. And of course, carrier mobility we are assuming that it is a constant thing, in reality does not turn out to be constant there is some dependence with the gate voltage, but for our purposes right now, we will neglect that.

So, with the gradual now, this is the gradual channel approximation and how do we you know, what is the current now drain current.

(Refer Slide Time: 22:33)

The way we can derive it is we will follow the similar approach, but we will make one small change. Now drain current is Q inversion divided by the time taken for it to travel the charge to travel. Now, I will say that Q inversion is not a fixed number. It is a function of position. And how do I capture the variation of inversion charges as a function of x? Well, I will write it as an aisle include Vx. So, I will say Id:

$$I_d = \frac{C_{ox}(V_{gs} - V_t)WL}{\tau}$$

$$\tau = \frac{L}{V}$$

$$\tau = \frac{L}{\mu dV_x/dx}$$

- Vx = 0 at the source end, but as you go to drain and it becomes equal to VDS
- Tau is the time taken for the carrier to travel from left to right
- Field is going to change you know, because there is some sort of a nonlinear distribution of voltage. So, electric field now will turn out to be dvx divided by dx.

$$I_d = \mu C_{ox}W(V_{gs} - V_t - V_x)dV_x/dx$$

Now what I will do is? I will integrate both sides I will take the other side. I will say the integral of I D dx. if you want to complete to compute the total current, you have to do an integral.

$$\int_0^L I_d dx = \mu C_{ox} \int_0^{V_d} (V_{gs} - V_t - V_x) dV_x$$

$$= \mu C_{ox} W \left[(V_{gs} - V_t) V_x * \frac{V_x^2}{2} \right] from\ 0\ to\ V_{ds}$$

$$I_d = \frac{\mu C_{ox} W}{L} [V_{gs} - V_t] V_{ds} - \frac{V_{ds}^2}{2}$$

So, *this is the square law* current no square law theory we see. What it tells you is current variances the square of voltage. There is a small correction here. Let us understand this a little bit more. What happens when VDS is small? When VDS is small, second term is negligible. This implies you have the linear approximation like. We have already seen this linear region linear approximation for current we have been able to get the same expression.

So, that is sort of a validation for us. What happens as you increase VDS? As we increase VDS, we said that we get to a saturation point. That we define it as you know, in the textbook from the figure from the textbook it is defined as VDSSAT which is VGS - VT or sometimes we can also refer to it as VDSAT, saturation voltage. So, you have two regimes one is the linear regime. As you go to larger and larger drain voltages, you get saturation.

And then the current remains flat. It does not change. And if you use larger gate voltage, the current increases, this is V GS increases, current increases. That this is this picture is not quite accurate. We will have to, even though this is simply a qualitative picture, I will actually show you an exact number that exact drain current that is calculated for a 0.25-micron technology in a moment. So, this is a square law. Let us analyse that a little bit more.

(Refer Slide Time: 28:42)

So, what I will do is? I will take this expression. And now what we are saying is, if you just purely look at this expression, how will the current change with respect to VDS? So, let us say let us try to plot ID versus VDS just based on the equation. What does it tell you? When VDS is small, the current increases, that is good when we would like that. But as you go to VDS higher than VD SAT then the second term takes over.

If you are just purely look at an expression, this is VDS square, this starts becoming dominant and this becomes dominant, the current starts reducing. So, if you look at purely the expression, the current should reduce like this which is not what actually happens. So, when we write this expression, we are implicitly saying that this is for VDS less than VDSAT. And what is VDSAT? We said just once again VGS - VT is VTSAT. This is equal to VDSAT = VGS - VT.

If your drain voltage is less than VDSAT set then this expression is good, but if your drain voltage is greater than VDSAT what does this expression become? This expression becomes:

$$I_D = \frac{\mu C_{ox} W}{L}\left[\left(V_{gs} - V_t\right)V_{DSat} * \frac{V_{DSat}^2}{2}\right]$$

$$I_D = \frac{\mu C_{ox} W}{2L}\left[\left(V_{gs} - V_t\right)^2\right];\ \ In\ Saturation$$

So, that and you see that as you increase the gate voltage, the current is increasing in square. Current increases as the square of gate voltage. That is why we call it the square law. So, the theory predicts that if you have a drain current like this.

And if you increase gate voltage, I will change it from V GS = 0.5 to 1 volt then my current will increase by saturation current will increase by 0.5 square. Well, it turns μ, C_{ox} are the process parameters $and\ W/L$ is what we can design.

So, the whole thing is you know, kind of fixed, so we will call this as transconductance parameter. We will discuss that in greater depth next week or next lecture maybe. So, here is what you have. Now, let me take an example. Let me try to calculate what happens to the drain current. I will take a simple example then after that can stop this video and then I will continue the next video.

$$I_D = \kappa[(V_{GS} - V_t)V_{ds}]V_{ds} * \frac{V_{ds}^2}{2}$$

So, I will ask you to calculate the drain current when let us say kappa = 1 amps per volt square V GS equal to, I will give you VGS -V T = 0.5, VDS = 1 volt, I will give you this expression, then I will ask you to calculate.

Many at times, whenever I teach a course of let us say 50 students or 80 students, at least there will be 5 to 10 students who will do this. What they will do is? They will substitute so ID is going to be:

$$I_d = 1 * [0.5 - 0.5] = 0$$

The answer there is no current which is flowing in the MOSFET which is not true. This is a kind of a small trick question. We should remember that now VDS is greater than VDSAT.

So, we have to change the current expression, we have to take VDS, we have to say

$$I_D = \frac{\kappa}{2}[(V_{GS} - V_t)^2]; for\ V_{ds} > V_{dsat}$$

I think if you do this calculation VGS - VT is now 0.5, 0.5 whole square will be 0. 25 divided by 2 will be 0.25 amps. This will be the correct drained. But many times, I will always find you know, students who will actually give me an answer 0 and 0 is going to be wrong.

So, this is what square law is and we will solve a couple of more examples, and we will discuss how NMOS and PMOS devices differ in the next video. So, I will see you there. Thank you very much.