Introduction to Semiconductor Devices
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Lecture - 58
Operating Modes of a MOSFET

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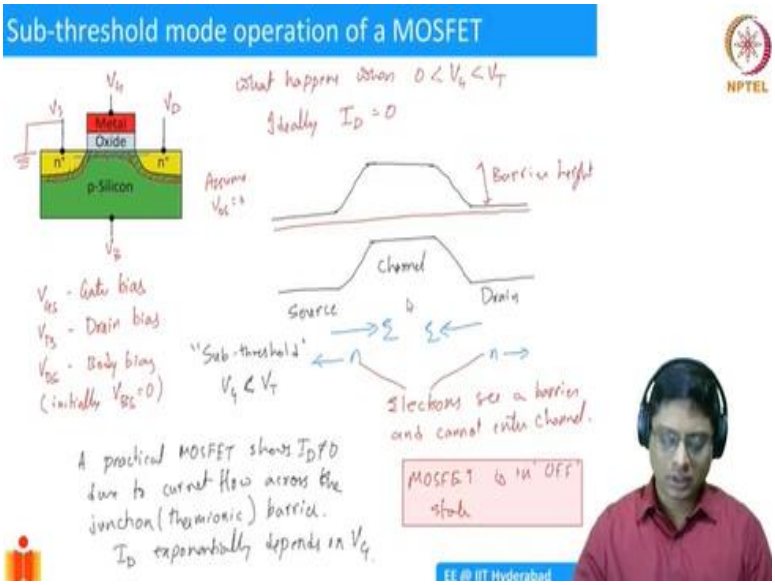

So, now we would like to talk about the various operating modes of a MOSFET. So, we have seen the structure of a MOSFET. Before we talk about operating modes, we need to label the biasing conditions. So, we have these four terminals. So, we can talk about the voltage in each of the terminals. So, gate voltage, drain voltage, source voltage and bulk voltage. Typically, what we do is we take source as a reference. So, what we will refer to is V GS.

So, this is typically what we will use. So, what we end up doing is in case of a NMOS device we ground the source and then we talk off the gate voltage related to the source voltage. So, this I will call as the gate bias and then V DS is basically drained bias and we could also talk about V BS which is you can apply voltage to the bulk also. That has some interesting implications. We will talk about it later on.

So, this is basically body bias you can say body bias. But right now, in the initial discussion we will take V BS = 0. If you do not say anything about the body voltage, you can assume that it is grounded for nMOS devices. So, once you have this, you know you have essentially two bias two voltage sources, you can change the gate voltage, you can change the drain voltage. So, what happens when you change these things?

So, the first thing we want to ask is what happens when V GS less than V T? There is no inversion charge, we may have depleted the MOSFET. Before we do that, let us say so this is a pn junction, so remember, there is always a depletion region here. So, this would be a depletion region. I am drawing it like this because it is an n + device.

So, the depletion region will be mostly in the body, very small amount should be in the n + regions, there is a depletion region. Now let us say apply voltage which is let us say I will write it as when V G is greater than 0, but less than V T. Then you end up having a small depletion region under the oxide as well you have the depletion region like this. So, now what do we expect in this voltage regime?

Well, there is simply a depletion but there is no inversion charge. So, there is no connection between the source and the drain. So, do we expect any current? Well, ideally, I D = 0 because V G is less than V T. But what happens practically? We have to understand how the current flows between the source and the drain and we will do that by drawing a band diagram.

We will try to draw a band diagram from source to drain. So, first, I will start with a Fermi level which is uniform. I do not have any applied voltage right now. Assume right now V DS is 0. There is no applied voltage across this. So, how do we do? Thus, the recipe for trying to find a job is always very similar, same. So, first draw other regions away from the junctions.

So, away from the junction this is an NMOS n + so it will be Ec here. There is let us say some bandgap. Similarly, on the other side, there is going to be another semiconductor like this and then in between them well, there is a p type semiconductor. Let us say, let me put it like this. This is how semiconductors behave. So, this is my source, this is my drain and in between there is a channel region. So, I am drawing the band diagram across the channel.

How do we connect this? Well, we have to connect them in such a way that the bands know the bandgap is maintained right there is nothing much here. So, you should be connected like this with this other side we should be connected with this. So, now if you look at this, how do the carriers flow in this structure? Well, here the electric field is this direction.

Because it is a positive slope, Ec bending in the positive has a positive slope whereas here the electric field is opposite direction. The drain and the junction negative slope so it is opposite direction. So, how will electrons move? Well, in this case electrons will move back, it cannot cross so electrons see a barrier. Similarly, here electrons will tend to go in this direction.

So, basically, what happens in this structure is electrons see a barrier and therefore cannot enter channel. But still you know, we always know that there is going to be some tunnelling across the barrier and all that. So, mainly what happens is the current that can flow is dependent on the barrier height. So, this is my barrier height. So, what we are saying is in our ideal MOSFET if your gate voltage is below the threshold voltage, we call it subthreshold operation.

So, subthreshold means V G less than V T for the NMOS device we have to take the profit convention. So, it will be below V T in the negative sense, 0 to -V T between that if it is there, it is a subthreshold operation for PMOS. So, now, once you have this in ideal MOSFET ID is 0 but in actual MOSFET in a practical MOSFET shows ID not equal to 0 due to current flow across the junction barrier or across we call it a thermionic barrier.

So, in this sort of a structure where you have this barrier, the current flow is basically exponentially dependent on the gate voltage, ID exponentially depends on VG. This is an important characteristic; it reduces exponentially with gate voltage in this case for NMOS device. We will talk a little bit more in depth when we show you the current voltage characteristics.

So, right now, I want you to understand that whenever your gate voltage is below the threshold, there is small amount of current, ideally, it was 0 but usually it is a small amount of current. So, the device is off. So, basically, sub threshold implies MOSFET is in OFF state. Well, what happens if you increase the gate voltage above VT?

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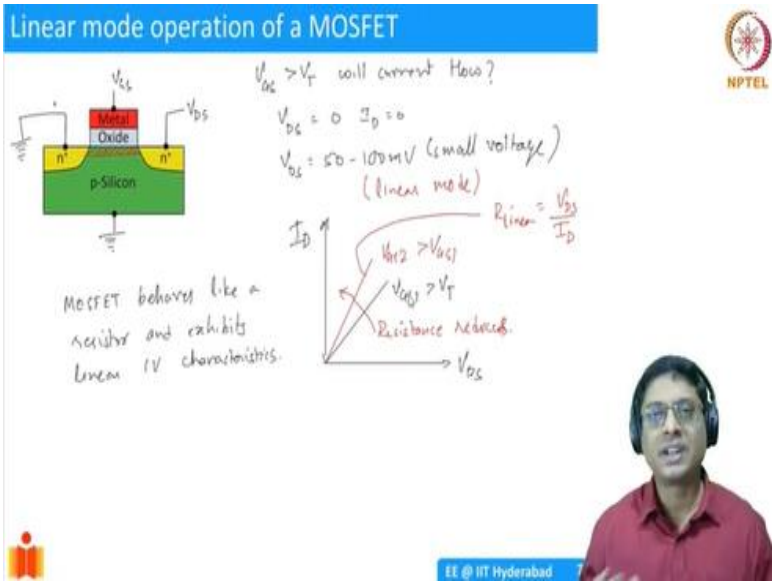

So, now let us consider the situation where I will say VGS is greater than VT? Well, you know I did not show you all the voltages but anyway now we understand what this, this is source is and we said this is usually grounded. Let us assume this also is grounded because we V BS is 0. Let us say this is connected to a VD or you can call it VDS, I mean the sources is 0 so VD or VDS is same, this is VGS.

So, now gate voltage is greater than the VT. So, there should be an inversion charge. So, will the current flow? The answer is it depends on the drain voltage. If VDS= 0, then essentially the more there is no voltage to make the current flow, you just have charges. So, ID = 0 but if VDS let us say like 50 to 100 mV. What happens?

Current can flow. And what will happen is we will derive an expression for this, but when you have VDS as small voltage like this, we call it a linear mode of operation. The reason we do that is if you let us say plot ID versus VDS. Initially when there is no voltage ID is 0, but the moment you start increasing VD the current starts increasing.

Since you know we have an integration charge anyway the VG has been fixed above VT. So, there is some current you know, depending on the gate voltage it will simply flow. So, we have basically let us call this as VGS1 greater than VT. So, current increases. Now if I increase the gate voltage what happens? Further increase the gate voltage for example, I make my issue of VGS1 and make it even higher than VGS1.

Then we are increasing the amount of charge here. So, we are making more inversion charge available, so the current increases. So, if I increase the gate voltage further you might have a situation like, VGS 2 is greater than VGS 1. So, effectively we are controlling the resistance of a MOSFET and the resistance is simply following the ohms law. So, if you look at this situation, the resistance is simply going to be R linear which is going to be simply VD by ID.

So, as you increase the gate what is the resistance reduces. So, you have higher current. So, this is how current the MOSFET behaves basically, whenever you have VG greater than VT and VDS has to be a small voltage 50 to 100 millivolts, MOSFET behaves like a resistor and exhibits linear IV characteristics. So, you can call it this as some resistance R_{linear}.

$$R_{linear} = V_{ds}/I_{ds}$$

But right now, I want you to understand the operation into doing. We did this so, now we are able to turn on the MOSFET. What happens if I increase my V DS still further?

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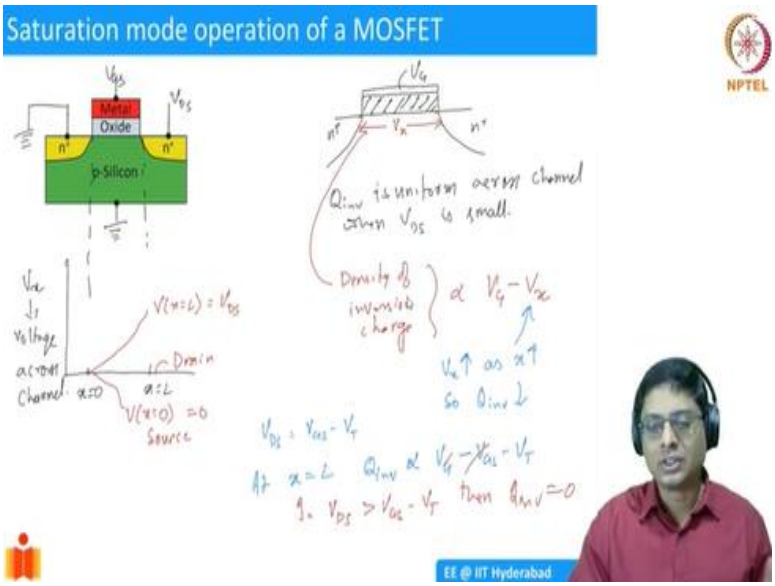

So, if you do that, VDS is large. Then we enter what is known as saturation mode of a MOSFET. To understand saturation mode let us do this. So, you have this to be grounded. You have VDS here; we have a VGS here. So, what is the voltage from source to drain? So, let us try to see if I can call this as, x = 0. That is the edge of the source region.

The junction between the source and the channel that will call an x = 0, the other one and call us x = L. The question is, what is the voltage between them across the channel, basically? So, I will call this as V of to be of x. So, this is simply voltage across channels. What do you expect

it to be? Well, when VDS was small, it is almost equal. I mean, this is you know there is negligible change in the voltage.

But the moment there is a large VDS, the voltage actually varies across the channel and takes a form, which is something like this. V (x=L) = VDS and V (x = 0) = 0, source is grounded. So, at the left edge of my channel, I should have 0 voltage at the right edge I should have a VDS in between them they could be linear approximation. You could even do that.

But it turns out it is not exactly linear here. I am not justifying why it is, but it is quadratic behaviour. And you have this voltage across the channel. x = L means it is drain and x = 0 means source. Below x = 0 its all source. There is a voltage drop so what? Well, to understand that we need to look at the inversion charge the amount of inversion charge. So, what we are having is let us say an oxide and there is a gate VG.

This is an oxide in between. So, what is the amount of Q inversion charge? So, you have this sort of structure n + n +, so what is the inversion charge? We assumed now that Q inversion is actually uniform across channel. When VDS is small, you just have a gate voltage and you are applying bulk was at the same potential so we did not really have much of a problem. But now what you are seeing is this voltage across this channel here, this is Vx.

So, if you had a Vx like this, what happens? So, the amount of inversion charge will vary across the channel. For example, at the left hand, what is the density of the inversion charge? What is it dependent on? Well, it is proportional to how much gate voltage I have but it is not just that but it is going to be a function of x. Because Vx voltage at that particular just below the gate oxide. Why is that? You could think of the entire oxide as tiny mass capacitor.

Each of them having a different voltage on the second plate. The top plate metal it is all uniform gate voltage, but in the bottom plate it is a semiconductor which is depleted so there is going to be some resistance and we are now applying a voltage across the channel. So, there is going to be variation of voltage across the channel. Because of which, the density will actually reduce as you go towards the drain side because Vx is increasing.

So, this Vx is basically channel charge voltage. So, Vx increases as x increases. So, Q inversion reduces as you go towards drain region. Similarly, you could think of what exactly should be

the voltage we would like to analyse. We will do that in a moment. So, this is an important part. So, if I have to draw, let us take an example and let us say may VDS = VGS - VT. I choose this specific number for a particular reason. It will become clear in a moment.

So, if my VDS = VGS - VT. What is the voltage which is applied across the capacitor, x = L at the drain edge my voltage which is sustaining my Q inversion, Q inversion is going to be proportional to VG – Vx. But now what is the Vx? It is VGS - V T. So, now what happens is, if your voltage is above that, you know if your drain voltages above VGS - V T then effectively there is no inversion charge at the drain end, you see this is going to cancel out.

If you are still further increase VDS so, this term will increase further. VDS is greater than VGS - VT then Q inversion is equal to 0. Because the threshold is where you have to Q inversion but below threshold there is nothing. So, essentially the effective gate voltage becomes less than VT and so there is no inversion charge.

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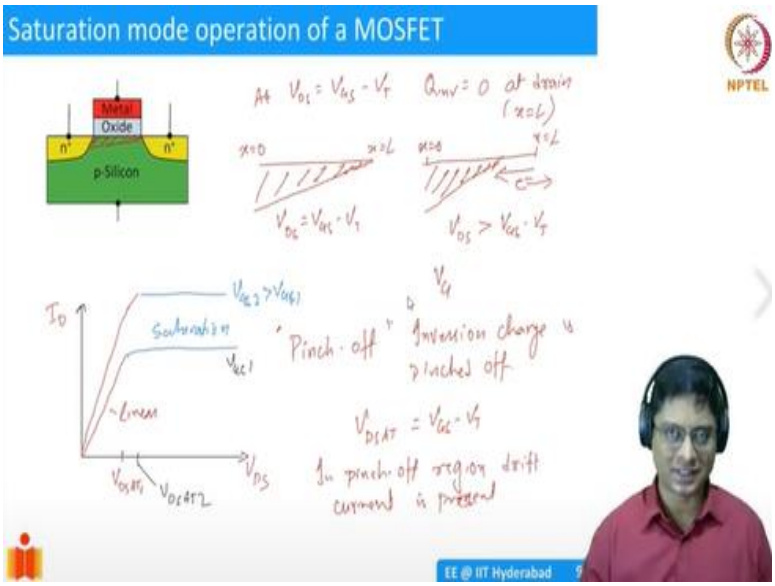

So, this I can schematically illustrate by drawing a structure having inversion charges like this. So, as my VDS increases, there is a variation of inversion charge across the channel. At VDS=VGS - VT, Q inversion is going to be 0 at drain or rather x = L. If you further increase VDS, what happens is let me just draw, so this is my Q inversion, this is my x = 0, x = L. This is at V DS = V GS - V T.

But I further increase my drain voltage then I will have a scenario where I will have it like this. This is my x = 0, this is my x = L, why is this happening? VDS is greater than VGS -VT. So,

the VG, basically you needs a voltage above the threshold voltage to sustain the inversion charge. So, that becomes less than VT and because of that, there is no inversion charge. So, this phenomenon is known as Pinch off.

Basically, the inversion charge is pinched off. So, what happens when you have pinch off? Well, in this case we will have, so let us say initially we have seen in the IV characteristics. So, if you call this as ID, this is VDS, there is an increase, there is a linear mode of operation. But once, let us say this is VGS - VT. So, once you cross that threshold, you know this way is a very, very special thing we will call it as VDSAT.

So, I will give a VDSAT = VGS - VT. VDS = VDSAT then your channel has got pinched off. So, after that the current cannot increase because effectively you know. Even though I am showing you, as if the charge is actually spatially non-uniform, it is effectively just a density of charges less. So, after that, there is no further charge that is being added by the gate because of that, the MOSFET enters into what we call us saturation region.

This is linear. So initially, the current will be linearly varying with the drain voltage. But once we cross VDSAT there is no further addition of inversion charge. In fact, the inversion charge is actually getting for a small distance here; near the drain physically it will be in this area, there is no inversion charge at all. The channel has got completely pinched off there is no inversion charge, because of that the current cannot increase any further.

So, whatever is inversion charge here that will cause the current to flow. Why will the current flow? Well, even though there is inversion charge, there is some field here which is going in opposite direction. So, electrons can still travel on this side, they will reach the drain they will get drift. So, in the pinch off region drift current is present.

When you have current, we have inversion charge it is still the drift, because V DS is supplying all over electric field, which will cause the carriers to go from the source to the drain. So, this is saturation. So, now if I increase my one VGS, let us say call this as VGS1. Now, what happens if I increase my VGS? Well, I will still have the same thing like this, but at a higher voltage and start seeing saturation, which is VGS 2 greater than VGS 1.

So, this is VDSAT1 VDSAT2. So, essentially, drain voltage at which reaches saturation will be higher because the VGS has increased, VDSAT = VGS - VT so it will increase because we have a higher number of current regions flowing through. So, these are the 3 main modes of operation of a MOSFET. So, the subthreshold regime where ideally it is 0, but practically it is going to be exponentially dependent on the gate voltage.

We will see the exact dependence later on. In the linear mode, the current is directly proportional to the drain voltage. The saturation mode; where if you increase V DS, it is not going to lead to any change in the drain current. So, these are the three main modes of operation of a MOSFET. So, this is a phenomenological or qualitative explanation of various modes.

We will actually derive the current expressions in the next lecture. So, I will see you there. Thank you so much. Bye.