Introduction to Semiconductor Devices
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Lecture - 8.5
NanoHUB Demo - MOS CV

This document is intended to accompany the lecture videos of the course "Introduction to Semiconductor Devices" offered by Dr. Naresh Emani on the NPTEL platform. It has been our effort to remove ambiguities and make the document readable. However, there may be some inadvertent errors. The reader is advised to refer to the original lecture video if he/she needs any clarification.

(Video Starts: 00:13) Hello, everyone. Welcome back. So, this is a brief demonstration of CV characteristics on Nanohub. So, I just lost into the MOSCap tool on Nanohub. By now, you should be knowing how to do this. So, let us play around with a few parameters and see what happens. So, let us before I run the first simulation, I just want to make sure that I change my initial voltage to 5 volts.

So, I want to see from -5 to 5 volts. And let us leave everything else at default and run it. So, you will get the first CV characteristic. So, we see that red curve is a LF CV and blue curve is a HF CV. So, we saw that you know the characteristic pattern that we explained in the class in the lectures you see this.

So, this is the normalized CV. So, capacitors make oxide capacitance. If you want to look at the standalone capacitance you can also see that. So, you see that it is about I would say 30 30, 35 nano-farads also. So, this is 30, 34 nano-farads at this point. And then you will see that in the inversion you have the flat CV characteristic high frequency CV characteristic. And notice that the threshold voltage is close to 50 millivolts in this case.

So, now, if I change my gate. So, this was p type substrate with n plus poly. I say no I do not want to use it, I use p plus poly so, that the work function is minimized. ϕ_{ms} is going to be small for this case when compared to ϕ_{ms} of n plus poly and p type. Please you know draw the energy levels and verify that what I am saying is correct. So, I will choose p plus poly.

So, what do you expect to happen? Well, now, there is a very small phi_{ms}. And there is going to be some contribution to VT from the Q_d/C_{ox} and the $2\phi_f$ term, surface potential term. So, if you simulate it, check it out. Well, if you want to compare, you can go to this all results so that you know both of them are plotted. So, this is the first simulation where I used n plus poly and p type.

The second simulation is where I am using p plus poly and p type. You see that there is a shift. So, the first one we saw the VT was around 50 millivolts. I am just taking the point where it is starting to go up. So, 50 to 80 millivolts but when you look at the second simulation where I use p plus poly, the VT is about 1.2 volts. So, you see this VT shift. You should be able to explain, why this is happening?

So, essentially, the ϕ_{ms} was negative and in the case, when I am using n plus poly and a p type substrate and that is actually pulling down the overall magnitude of VT. You could do the same thing with even p MOS. So, I will use an n type substrate. Now, let me run with p plus poly. So, we would expect the shape of the VT to change. Is not it? It is p MOS. So, you see this is your p MOS device and the VT is again around the same point.

But if I use n plus poly, I do not care about the impact of ϕ_{ms} but I just want to minimize ϕ_{ms}. If you do that, you will choose n type and n plus polysilicon. If you do that it turns out that it would not be the good thing to do. You see here. So, this is your width n type substrate and n plus poly. And this is your p type substrate and p plus poly. So, both these occasions you know, the magnitude of VT is higher.

Whereas if you choose n plus poly and p type substrate and p plus poly and n type substrate, you see that the VT's are very close to each other and very small number. This is very important. That is what I wanted to emphasize once again. Let us clear this up now. And let us study one more time. Let us that is n type and p plus let us choose p plus polysilicon and then run the simulation.

So, this is what you have a p MOS device so that it is switching on. I mean or rather it is going into inversion when you have negative voltages. Now, instead of polysilicon gate, I will choose

aluminum gate. What would happen to this? We need to plot both. You see here. There is already a significant shift towards the negative voltages.

This essentially means that there is some small depletion probably happening at 0 volts whereas if you take the earlier case of p plus poly and n type substrate. You saw that there is already almost like a close to inversion happening close to 0 without any applied voltage. That does not happen with metal. Great so, where are there are various options that we can analyze.

You know when we do the device design. There are many constraints that we need to understand. So, this is the first step in understanding. So, now I will clear again this one. I will go back to my p plus poly. Keep it. And quickly load the result. Now, what happens if I reduce my oxide thickness? You could check that out by increasing the oxide thickness and simulate it.

So, we saw that in the inversion the capacitance was going up. But you know that is the normalized capacitor that I showed in the lecture. So, because the oxide capacitance also should change, because we are changing the thickness of oxide. So, if you are having this is the original simulation with 0.1 micron thick and then the second simulation with 0.3-micron thick oxide.

And of course, you know we saw that why the VT shift was happening. You know we explained this in the class. But it might be perplexing to you that, why is oxide capacitance is not changing? The reason it is not changing is this is a normalized curve of capacitance by oxide capacitance. If you want to look at the actual capacitances, I could plot this. You see here. So, this is with oxide thickness of 0.1.

And if I increase my oxide thickness, the oxide capacitance is actually dropping significantly. It is not the same anymore. So, there is a significant difference between the 2. And you see that if you look at both these CV characteristics, what do you conclude about the effectiveness of the gate? So, we say the gate is very effective when it is able to have a significant difference between the oxide and inversion capacitance.

And, by that measure we will see that 0.1-micron thickness of oxide is much more efficient than 0.3 micron because it is able to switch it quiet, there is a switch if you call this as on state and this is off state. So, we will introduce this in more detail later on. You will see that there is

a significant change in the capacitance. So, we were able to control the inversion charge much more effectively.

That is why even the VT is smaller. So, because we are able to create the inversion charge very easily. You could also try you know what happens if I change my dielectric constant. I will stay at 0.3 micron. But I will increase my dielectric constant. Let us say 3 times. I will make it 12.

I mean there is definitely some materials which will have dielectric constant of 12. By the way, you might ask you said that you know dielectric constant of high k hafnium dioxide was 25 and silicon dioxide was 33.9. How are you able to capture all the material properties with a single number? Well, for that you have to actually do the studies of polarization.

You can actually capture the electric response by just one number here, dielectric constant. Especially you know when magnetic response is not important. Now, we increase the dielectric constant by 3 times. Let us see, what happens? So, this is your third simulation with dielectric constant of 12 whereas second simulation was this.

This is basically with dielectric constant of 3.9. But if you go back to the first case, it is again back here. So, essentially what this tells us is I can increase my oxide thickness if I am simultaneously increasing my dielectric constant. This is the advantage of using high k dielectric. You can still retain same capacitive control. So, let us do it one more time. Just you know I will clear up so that it is much cleaner.

So, I will say the first option was I wanted to make my oxide thin. So, I will make it 0.1 micron and I will keep the directive constant as 3.9. I will simulate. I have this initial result. Now, let us say I could even try with 0.01. I wanted to make it thinner, 10 nanometers. You will definitely see a much stronger oxide capacitance. LF CV is having some issues.

This is with 10 nanometer oxide. This is with 100 nanometers. So, you have a much stronger gate control. Effectively, this is becoming behaving more like a perfect capacitor. So, it is immediately going back up. So, in an ideal parallel plate capacitor you would expect it to be constant. So, we are trending to that behavior. So, now say let us say I have a lot of leakage which I want to decrease.

So, what I could do is simply increase this. You know I can increase this by let us say I will make it twice you know 7.8. I will go back to 0.1um. So, essentially, I am now having a better gate capacitance. So, I should get a better control on the inversion charge. So, you will see the difference in a moment. Yes, this is 7.8.

So, you are able to you get a strong control. So, this is my initial simulation, let me plot CV characteristics. So, you have this sort of a control. Now, we tried actually decreasing it to 10 nanometers we have a very strong control. But without actually decreasing the thickness I could maintain the same 0.1 micron but increase the dielectric constant.

You see that there is a stronger gate control on the inversion charge. So, we can do a whole variety of simulations and analyze. So, this will give you a lot of insight. You know I just explored some of them. Let me just try it once. I will clear all. I will go back to my original standard configuration of 0.1 microns and 3.9.

I will just load the default simulation. And now if I add let us say a fixed charge. Let us add it and put $1e^{14}$. If you have this much of positive fixed stock set charge in a p MOS, you will expect the VT to be shifted you know more negative values.

Well, it is very small effect because this is still not a lot of charge. So, you have to have a larger volume of charge. Let us say 19. Now, it is volume charge, 10^{12} interface charge would have been enough. Something went wrong. This charge is too high. So, I should not have done that. So, I will clear this simulation.

And then now I will do instead of, 10^{16}. So, now, you have basically a shift in the VT. You can actually zoom in here. You see originally, we had this V CV. So, initially there was no charge 0 then we added 10^{14}. That was not enough. There is only a very small change. This is per centimeter cube. It is significant.

Generally, in the lectures, we talked about Q_i. That Q_i was per centimeter square. So, please notice the difference. This is for centimeter cube. So, this is much larger number. So, I need to

actually take a, you know power of 2 by 3. Only then I will get an equivalent surface charge. So, please do not put this number directly.

If you put this number directly into your calculation in the VT, you will really get very large VT. So, this is a volume charge. It is not a surface charge. In the example, in the calculations, we are taking VT as Q_i i.e., surface charge at the interface (equality interface charge) we mentioned. So, we have to be careful.

Anyway, so, that will all give you lot of you know lot of experience. So, you could change even frequency. What happens if I change my frequency? No, we did not discuss this. But this can be done. And you could study what happened. You just check it out. You should be able to guess it. So, in this way, there are lot of things that can be explored over Nanohub. So, I would strongly urge you to you know check it out.

And I did not change the doping now. But I have taken I have changed the doping and I have shown you what happens in the slides. So, please verify all these things. It will be a good way to analyze. You might ask why all this required you know. Well, you see the semiconductor world is a very rich and diverse thing. If you want to work in those industries, you have to have a strong basics. And this is how you develop.

And some of these things are not really covered in a regular you know undergraduate curriculum. I understand that. But I think whoever so interested in the depth I think should definitely spend some time. Thank you so much, bye. **(Video Ends: 18:49)**