Introduction to Semiconductor Devices
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Lecture - 8.4
Impact of Doping, Oxide Thickness and Temperature on CV

This document is intended to accompany the lecture videos of the course "Introduction to Semiconductor Devices" offered by Dr. Naresh Emani on the NPTEL platform. It has been our effort to remove ambiguities and make the document readable. However, there may be some inadvertent errors. The reader is advised to refer to the original lecture video if he/she needs any clarification.

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Hello, welcome back. So, in this video, I wanted to discuss a few ways to tune the main device parameters namely V_T. How do we design a MOS device? So, that it has a certain V_T and you know, what are the various parameters that impact V_T? And, how do the you know how do the CV look like when you change let us say doping? When you change oxide thickness, what happens to the CV?

So, that will help us understand how the device works. So, let us go back to the basic structure. We were talking about a basic assembly, so, I will just make it like this. And then there is a oxide on top. This is my and there is a metal on top of this. This is my basic MOS structure. So, this is let us say, some substrate. Let us say we have N_a. This is my t_{ox}. So, if you calculate this I mean if you measure the CV or such a device, you apply for I mean we discuss a circuit, how to do this?

If you do that, what you end up getting is let us say a CV which looks like this. So, you have this C_{ox} and this is C_{min}. And of course, what happens when you know this is your V_T. These are the 3 main parameters in the CV. So, how do these things behave? First thing we will ask is what happens when you have when you increase the substrate doping. When you increase substrate doping, will the accumulation capacitance or you know C_{ox} change?

Well, no, because the C_{ox} we saw was purely geometric.

$$C_{OX} = \frac{\varepsilon_{ox}}{t_{ox}}$$

purely geometric. So, this does not change with N_a. It does not change with N_a. That is good news, part of it. So, what happens to C_{min}? C, will C_{min} change with N_a? To understand that, what happens when you increase N_a? The substrate doping increases then the depletion width is going to reduce.

You do not need to uncover as much charge as much you know deeper into the sub semiconductor. So, depletion, $W_{depletion}$ reduces that implies that your $C_{depletion}$ is going to increase. Therefore, your C_{min} which is going to be

$$C_{min} = \frac{C_{ox}C_{dep}}{C_{ox} + C_{dep}}$$

this is going to increase because you know you see when you have this sort of a sum, it will be close to the smallest number always.

If the ratio is large then it will be almost equal to the lowest number. So, what happens when N_a increases? Well, it turns out that it increases in this fashion. C min increases . This is one thing that we will expect as N_a increases. Let us say, what happens if your oxide thickness increases? If your oxide thickness increases let me put it in the, so, t_{ox} increases, what should happen?

Well, one of the consequence is I mean straight forward consequence is C_{ox} will reduce. Capacitance of the oxide will reduce. So, this implies gate has weaker control. You do not really have a sufficient ability to deplete or invert you need to. So, it will be much weak weaker control. Essentially that is what it is. So, how does the gate voltage fall across the oxide and semiconductor?

So, V_G, we have seen is

$$V_G = -\frac{Q_d}{C_{ox}} + \Phi_s$$

. And this is essentially going to be V oxide. So, this increases because sorry C_{ox} decreases. So, V oxide increases. So, if you have the same voltage, then your Φ_s has to be smaller. If you for a particular voltage V_G for a particular V_G, t_{ox} increases implies Φ_s has to reduce because oxide is going to take a much larger fraction of the voltage.

So, if Φ_s decreases, what happens to the W depletion? The width of the depletion region is

$$W_{dep} = \sqrt{\frac{2\varepsilon_{si}}{qN_a}\Phi_s}$$

. So, $W_{depletion}$ reduces. That implies $C_{depletion}$ increases. So, basically again if you have even a same oxide thickness reducing t_{ox} increase, Na increases. Both cases, C min will increase.

So, this is what we would expect from a Cmin increases as t_{ox} increases. Well, you know this is what we would expect. So, what I did was I went to nanoHUB.

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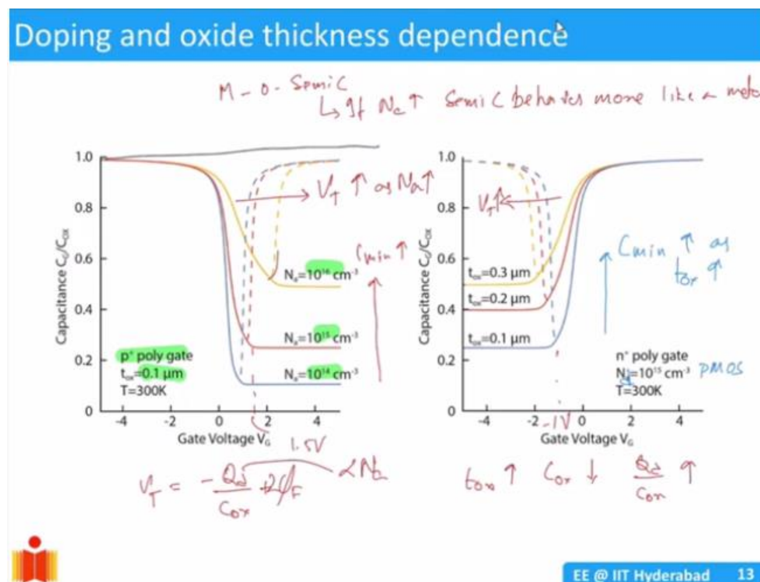

And then I grabbed a few CVs. You know I downloaded them and then plotted them cleaned up a little bit. So, this is what you get you know. So, I I use 3 different doping concentrations. So, 10 power 14 15 16 and then you run a same CV. So, in this case what I did was I took a

substrate thickness of oxide is 0.1 micron and p plus polysilicon . So, you yourself can actually verify this for yourself.

So, if you take 10 power you know let us say 10^{15} concentration, your V_T was somewhere you know around 1.5 volt or something. So, what you notice is clearly the C_{min} is increasing. This is what you were talking about in the last class the last slide. So, C_{min} increases. And in a way that is sensible because what does increasing the doping of the semiconductor mean. So, what you have is a metal oxide and a semiconductor.

Now, if N_a increases, semiconductor behaves more like a metal. Is not it? So, effectively you are kind of approaching the parallel plate capacitor sort of a structure. How does the CV of a parallel plate capacitor look like? Well, it will be flat constant. It does not change it is fixed number. So, as you increase the doping concentration you are approaching the parallel plate capacitor. That is one aspect.

The other aspects if you notice this point where you know the HFs you know this LF CV's charge is going up. This is basically threshold. So, V_T is increasing as N_a is increasing. Why does that happen? So, well remember, what is V_T?

$$V_T = -\frac{Q_d}{C_{ox}} + 2\Phi_F$$

So, Q d is basically proportional. This guy is proportional to N_a. As you increase the doping concentration, V_T is going to increase.

If you do not want a high V_T, you need to use a low N_a. But then if you have low N_a there will be some other side effects. We will when if you are actually doing the device design you have to take care of all these things. Then what happens to the oxide thickness dependence? We are again seeing the same trend.

So, basically C_{min} increases as t_{ox} increases. So, this was done with a slightly different you know I chose deliberately chose now well I wrote N_a here but that is incorrect. This should be N_d. This is a pMOS device. So, it has to be n-type substrate. So, N_d that is 10^{15} . It is and n plus poly. n plus poly over nMOS n-type semiconductor. So, you see that you know V_T is typically in the range of 1 volt.

I am deliberately mentioning this so that I will compare it you know. I will ask you also to compare. In the last video, we mentioned that if you use if you have an n-type substrate, use a p plus. And if you have a p-type substrate, use an n plus. That is the, another advantage is it lower the V_T, I said. So, you can verify that yourself. So, anyway as the thickness of oxide is increasing we explained this trend already.

And there is a small dependence on V_T again here. V_T in magnitude is increasing. Why is that happening? Well, if your thickness t_{ox} is increasing C_{ox} is reducing. So, your Qd/C_{ox} is going to increase. So, it is going to increase. But you see it is not that much of an effect as compared to N_a. It is much weaker effect. It seems to be that. So, one of the let us I will mention that again. So, now let us move on to the next thing.

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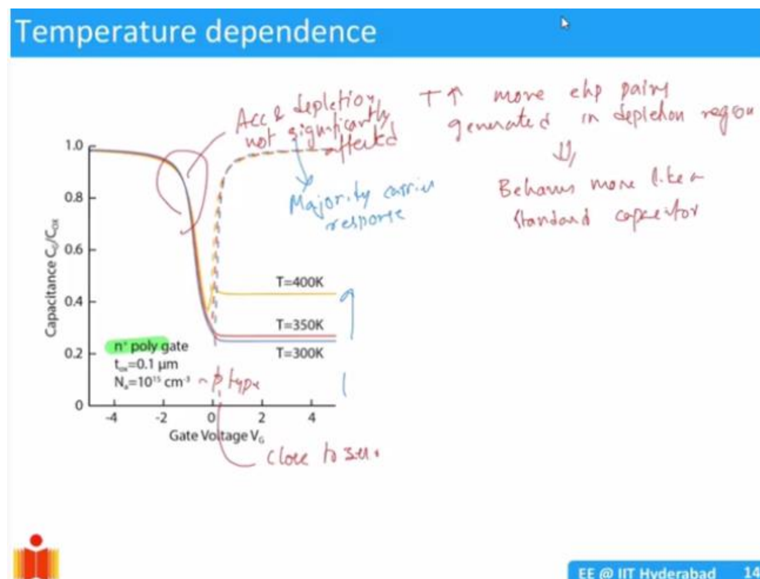

That is basically temperature dependence. This is again another thing that you can simulate a nanoHUB and check. So, in this case, deliberately I chose a p type substrate and an n plus poly. If I do that you will notice that the V_T is close to 0. I mean it will be 0.1 0.2 something like that. So, see the distinction when I use a p type and p plus poly, it will be it was 1 1.2 something like that 1 1.5.

But now if I use a n plus poly I am actually reducing the absolute magnitude of my V_T. And as temperature increases, as T increases, you have more ehp pairs generated. pH generated in depletion. So, if you have more ehp pairs, essentially this behaves more like a standard capacitor. So, it tends to go up. So, and also one important thing to notice here, accumulation and depletion not significantly affected.

Inversion is where you have the problem because inversion is the minority carrier response and if it is not fast enough we know how it behaves. So, inversion is a something that you have to always pay attention to. Here, because I said we also said this is because of it is dominated by majority carrier response. And they are quite fast in responding and this is how the temperature changes.

So, you see that you know as you go to higher and higher temperatures there is a very significant increase in the minority carriers. So, that tends to screw up your devices. So, that is why you know electronic devices whenever they get heated it is not good for their, you know lifetime. They goes they spoil and get spoiled much faster. So, whenever your laptop or computer is getting heated up aggressively then you have to really think about what is happening.

And it might actually be approaching the end of its life. So, this was the parameter dependence that I wanted to talk about. One last thing I wanted to just you know come back to before I stopped discussion of MOS capacitors is gate oxide scaling.

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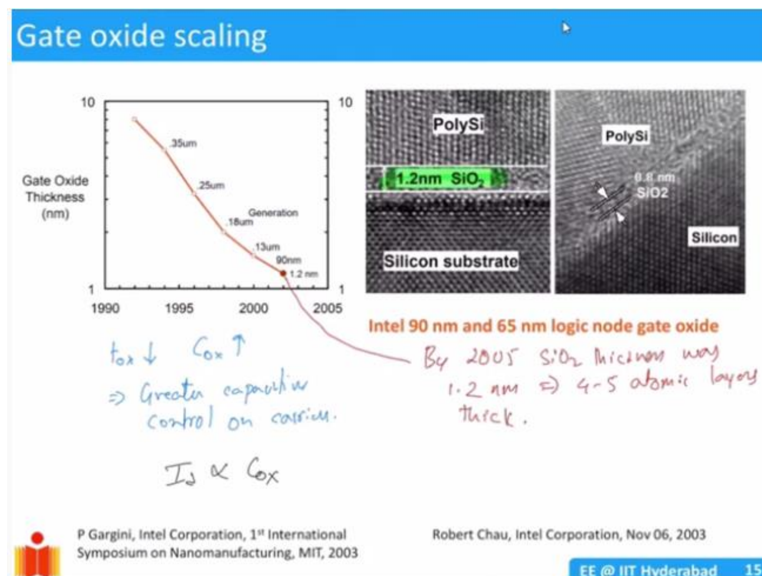

So, we saw that you know basically this slide I think it was in the first video on MOS capacitor I showed you this. And I mentioned that over the time the thickness of the gate oxide kept on reducing. The reason it was reducing is if your t oxide reduces C oxide increases. This implies that you have greater capacitive control on carriers. So, essentially we are you know we are eventually you know from next lecture we are talk next week we are going to talk about MOSFETs.

MOSFETs are essentially devices where you switch off current and switch on current. You want to have a very strong control on that. You do not want to you know have a weak control. So, one of the requirements was always to use C_{ox}. And we will see very soon in the next couple of lecture next week lectures that Id the drain current which is one of the important parameters in the MOSFET. That is going to be proportional to C_{ox}

So, if your C_{ox} is large your Id is going to be large. If Id is large then the transistor works faster. I mean it will essentially charge and discharge faster. So, this is one of the main effects. So, because of this over the last 40 45 years, scientists you know technologist have been scaling down the oxide thickness. So, now what happened was as you do this, by the year 2007, by I would say even 2005 excuse me SiO 2 thickness was 1.2 nanometers.

This implies that it is essentially you know 4 to 5 monolayers 4 to 5 atomic layers thick. I mentioned this fact already, layers thick. So, if you have very thin t SiO_2 as shown in the picture as well here so, this is a very thin thickness of SiO 2. And because of that you can have strong leakage.

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So, we showed the band diagram of a MOSCAP before. So, essentially you can have electrons which are tunneling from the metal into the semiconductor because this thickness is now 1 to 2 nanometers 1.2 nanometers whatever. So, you can have a strong leakage. Electrons tunnel giving rise to leakage current. What happens when the oxide leaks capacitor action is lost capacitor action is lost?

So, as we were talking so, when there is tunneling of electrons into the oxide through the oxide there is leakage current. And leakage current is going to spoil the capacitive action. So, how do we you know get around that? Well, we are having 2 opposite requirements. If you want to reduce tunneling, you need to have a thicker oxide. But if you want to have a strong gate you know capacitive action.

You have to have a strong C_{ox}. That means C_{ox} has to be large. That implies t ox has to be small. So, there are these 2 counterproductive things. And there is nothing much could that could be done till 2007. So, in 2007, you know Intel came up with this I mean the idea was there for a long time but practically Intel introduced the technology in 2007. What they did was remember, what is C_{ox}?

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

So, all the time, we have been reducing this, reduce t_{ox}. Till 2007, I would say. But then there is another lever that we have which is increase ε_{ox}. That also has a similar effect. So, what does increase epsilon oxide mean? Well, oxide cannot be you know oxides material parameters are fixed. We cannot do much about it. But it turns out that we can replace the idea is replace silicon dioxide with a high k dielectric.

What do we mean by high k dielectric? Well, it is something you know high dielectric constant essentially. So, this epsilon relative of let us say this is a example will be hafnium dioxide is one of the high k dielectrics is about 25. So, essentially, silicon dioxide epsilon relative of SiO_2 which we have been using so far is 3.9. So, instead of using 3.9, use hafnium dioxide instead of silicon dioxide.

That is what that was the approach that was finally demonstrated. It is been known since I think 90s early 90s. But finally, Intel managed to demonstrate it in 2007. They actually the Intel penryn processors 45 nanometer technology was actually based on this. So, we replace this by high k dielectric. So, what? Well, what it effectively lets you do is like let us imagine.

You know for same capacitive control, capacitive control, essentially I should have C_{ox} I mean the oxide capacitance or you know gate capacitance should be same. So, what I will do

$$\frac{\varepsilon_{ox}}{t_{ox}} = \frac{\varepsilon_{high-k}}{t_{high-k}}$$

. So, what this implies is I can quickly write

$$t_{high-k} = \frac{\varepsilon_{high-k}}{\varepsilon_{ox}} \times t_{ox} = \frac{25}{3.9} \times t_{ox}$$

So, in 2007, it was 1.2 nanometers it was not in 2005 it was 1.5 nanometer 1.2 nanometers. So, immediately if you just replace silicon dioxide with hafnium dioxide, you could have thickness of a high k to be about 6 nanometers. So, you are able to get a physically thick gate oxide and still have the same capacitive control same current. You know because C_{ox} is still the same.

So, this was the, you know it was a simple idea. But once you increase the thickness this you know tunneling quantum tunneling is avoided quantum tunneling is reduced just by using a different material. But well, it is not that simple because you know in the beginning of MOS devices itself I mentioned that one of the great features of silicon dioxide system was that the quality of the interface was very good.

So, there are very few defects. But the moment you use hafnium dioxide or you know there are a few other class of dielectrics all these high k dielectrics. So, if you use them, the interface quality turns out to be not so good. So, it required a lot of technological achievements to make sure that it works in real life. So, it is not a simple problem I am sure quite a few billion dollars were spent on this to actually make this process work.

But once it was achieved, the processors were able to go faster. The scaling continue, and we will talk more about it. This is what we know we would call as scaling. So, I will give you a small problem in the assignment based on the high k dielectrics, just compute some numbers. Or maybe one of these problems I will do it for high k so that you get an exposure of what it is. And then we will understand.

You know this is just one aspect of scaling. The thickness of the oxide is reducing. We will talk about other aspects once we discuss the basic MOSFET. So, now the plan is that in the next you know I will record one more, short video using you know showing you some CV examples from nanoHUB. By now, you should be comfortable. But anyway, I will just go ahead and show you a few things which I think are important.

You can either follow along on your own or you can try to explore and see what it is. That will help you. You know refresh the things that we are learning here. So, that is an interactive learning tool and I sort of I am fond of it. And I am I think it will be very useful. So, I will record that short video 10, 15 minutes or so. And then I will stop. So, that will be the end of the MOS capacitor discussion. And in the next week, we will start off with MOSFETs.

So, thank you so much for your attention. And I hope you are having a great time learning this. I will see you in next week, bye.