Introduction to Semiconductor Devices
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Lecture - 8.3
Example Problems with MOSCAPs

Hello, welcome back. So, in this video, we will solve a few problems so that we get better familiarity with MOS capacitors. So, in the last few lectures, we have understood what a MOS CV means and how it looks like. And you know, why? What is the physical reasons why it behaves the way it does? So, now let us try to solve a couple of problems. The first problem we would like to solve is this.

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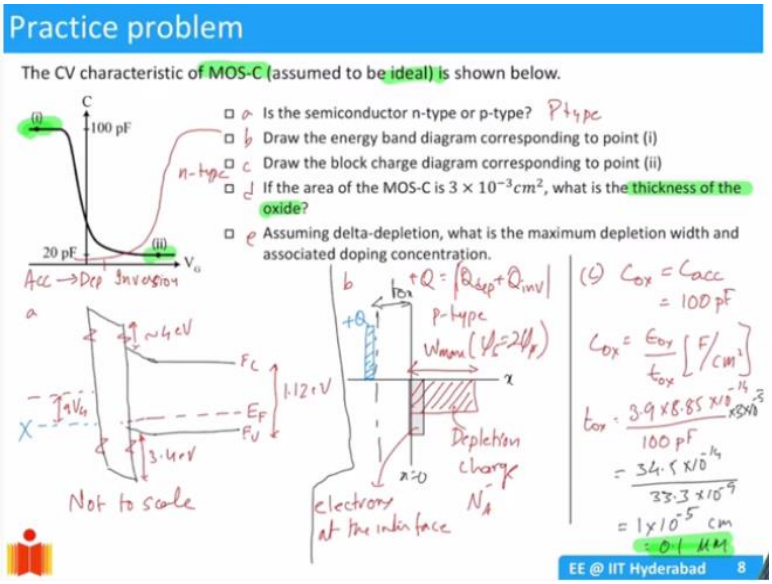

So, we are given a CV curve. And some you know two points the CV the capacitance numbers are also given to us. And this capacitor MOS capacitor is assumed to be ideal is an ideal MOS capacitor. So, there are a few questions here and we want to answer them one by one. So, first of all, when you look at the CV, is a semiconductor n-type or b-type? How do we answer that? Well, first, we have to identify, where is the inversion?

So, there is oxide capacitance accumulation capacitance and the inversion capacitance. So, from our understanding of the concepts, we saw that whenever the oxide is you know capacitance is involved it does not change its voltage. So, this part is the accumulation region. And then we go towards depletion. And finally we hit it you know at this point we hit the inversion. So, at positive voltages, we are having small capacitance smaller capacitance.

So, it looks like it is a p-type substrate because when you have a p-type substrate you apply a voltage then it creates a depletion region and then you will have inversion. So, it looks like it is a p type. So, you need to be able to explain, why it is p type? You cannot simply say that or wherever it is you know if your capacitance is lower in the positive gate voltages, it is p-type because I could have as easily a capacitance curve which looks like this.

Here also in the positive gate voltages, you are having the smaller capacitance. But this is not p-type substrate. This is an n-type substrate. So, the aspect we need to track is as you increase the voltage, what is happening to the capacitance? Here as we increase the voltage, it is increasing. So, this is clearly not going to satisfy the p type sort of behavior. So, that is why we need to be able to clearly explain. Why?

You know, from looking at the transition from accumulation to inversion, we conclude that it is a p-type semiconductor. Good, the next question is, draw the energy band diagram corresponding to the point 1. Well, your point 1 is here. So, clearly, it is an accumulation. So, the question is an indirect way of asking you to draw the band diagram for a MOS capacitor in accumulation. How would you draw that?

So, whenever we want to draw the band diagrams, first draw the bulk. For especially MOS capacitors, you can draw the bulk first. I will identify the bulk regions, this way. And we conclude it that it is a p-type semiconductor. So, I will put my E_F closer to E_V. This is my bands in the bulk. And now we are saying that it is an accumulation. So, what are accumulating? So, its majority carriers are p-type you know holes.

So, basically you are going to have more holes closer to the interface. So, I need to bend my bands slightly in such a way that. So, this is my accumulation of holes because if I extend my Fermi energy till here so, I have the distance between E_F and E_V reducing. So, that means there

are more holes. So, clearly the bands are bending upwards. So, after that almost you know without any thought you could draw that electric field will be in the same direction in the oxide.

We have seen that you know unless there is some you know charge discrete charge somewhere you know additional charge sheet. This will not change. We have seen in the charge block diagrams block charge diagrams. So, this is how it is. And now, what happens to the Fermi level in the metal? Well, we are applying a negative voltage and we are reaching accumulation.

So, E_F cannot simply be at the same level. This will be wrong. This is without any voltage. So, this will be wrong if you draw E_F of metal here. We are applying a negative voltage. So, if I apply a negative voltage, E_F is going to shift up. And this difference is going to be q times V_G applied voltage. So, this is how a band diagram looks like you know. Of course, you know always this is not to scale. We remember this always.

We are only showing the essential physics because this distance is going to be 1.12 eV band gap of silicon. And this we saw was close to 3 eV or even 4 eV. Electron affinity was close to 4 eV for silicon. And this is close to maybe 3 to 4 eV. So, we are not drawing it to scale. But we are showing the essential physics. That is all. One way of representing that you know we are not trying to scale with would be to put something like this.

This mark indicates that there is a break in the axis there. So, this is how a band diagram will look like in accumulation. You should also practice how the band diagram looks like in inversion. Please do that. It is helpful for you. Now, let us the third question is draw the block charge diagram corresponding to the point 2. Well, point 2 is here. It is clearly an inversion. So, how does the block charge look like?

To draw the block charge diagram in inversion, what I would need is, I will, based on the basic axis, let us say this is my x. And I will assume that my, this is my oxide thickness. So, this is, I put a straight line there. So, I will call this as x equal to and this is x equal to 0. So, this thickness I will assume that it is t_{ox}. So, now clearly we are having inversion. So, what does it mean? We are also applying positive voltage.

So, there should be a positive charge on the gate and that will be right at the interface. I cannot emphasize this enough. Whenever we draw as thin line like this, it essentially means that set

the interface. This is my plus Q. What is this gate voltage doing? You know positive gate voltage is pushing the holes away from the interface. So, on the semiconductor side, this was a p-type semiconductor. And we push away the holes.

What remains is a exposed acceptor ion. So, that is why I should get. This is my depletion charge, so, depletion charge. How is this form? This is basically N_A minus. So, you are pushing away something. And by the way, since, it is in inversion, what will be the thickness of the depletion region? This region is going to be w max, maximum depletion width. How much is the maximum depletion width?

Well, that is a width when you calculate the width corresponding to surface potential of 2 phi F. When you do that you get the maximum depletion width. Is that all? Well, no, we are not at threshold. We are actually much beyond threshold. There should be a substantial number of inversion charges. The inversion charges for a p-type semiconductor are electrons. So, I need to show my inversion charge here.

So, I will draw a, so, structure like this. Basically, this is showing you that these are electrons at the interface. So, overall your plus Q whatever you have Q, plus Q should be equal to Q depletion plus Q inversion. The sum in the in terms of magnitude, they should be equal. Both are negative. So, sum it up. That should be the charge balance. Always the charge balance has to be maintained. There is no other escape from that.

It is one of the fundamental laws of physics. Fine, so, this is done. How about the next part? You know, if the area of the MOS capacitor is $3 * 10^{-3}$ cm^2, what is the thickness of oxide? Why are we given area? So, well the reason for that is, we know, what is oxide capacitance? Because we know what is the C in the accumulation

$$C_{ox} = C_{acc} = 100pF$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}\left(\frac{F}{cm^2}\right)$$

$$t_{ox} = \frac{3.9 * 8.85 * 10^{-14} * 3 * 10^{-3}}{100 * 10^{-12}} = 0.1\mu m$$

And the last question is assuming delta depletion, what is the maximum depletion width and the associated doping concentration?

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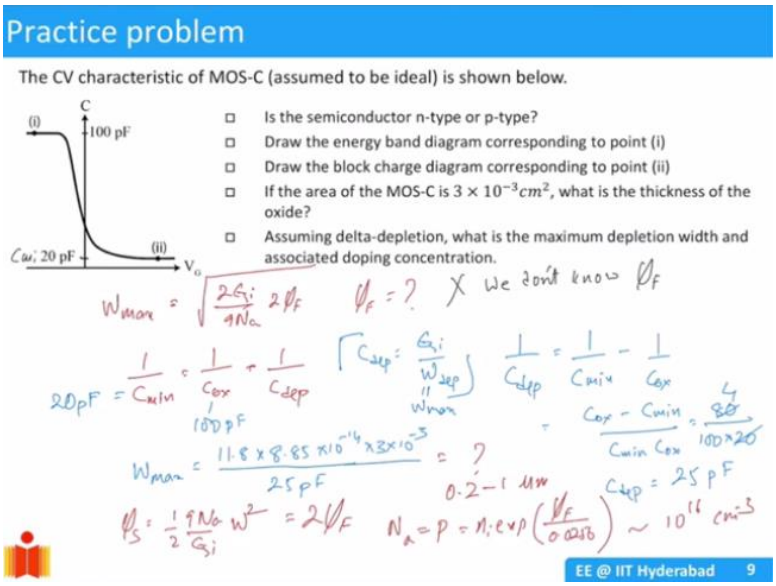

$$\frac{1}{C_{dep}} = \frac{1}{C_{min}} - \frac{1}{C_{ox}} = \frac{C_{ox} - C_{min}}{C_{ox}C_{min}} = 25pF$$

$$C_{dep} = \frac{\epsilon_{si}}{W_{dep}} = \frac{\epsilon_{si}}{W_{max}}$$

$$\Phi_s = 2\Phi_F = \frac{qN_aW^2}{2\epsilon_{si}}$$

$$N_a = p = n_i exp\left(\frac{\Phi_F}{0.0256}\right) = 10^{16}cm^{-3}$$

We are almost there. You should be able to solve this fully. So, that is the first problem I wanted to solve.

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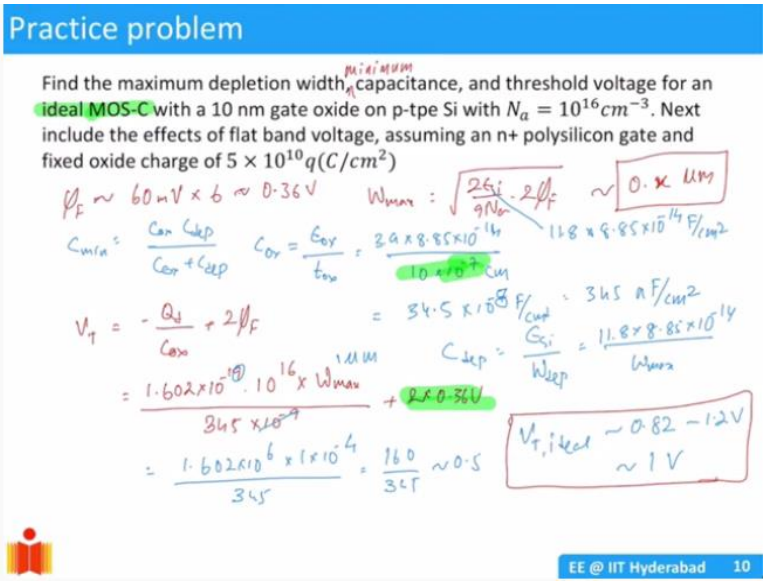

And I quickly want to solve the second problem. So, this problem is, find the maximum depletion width. And you know, let us call this as minimum capacitance. And threshold voltage for a ideal MOS capacitor with some 10 nanometer gate oxide and p type silicon. And Na is given to us which is good. And then include the effects of flat band voltage assuming n plus polysilicon and fixed oxide charge.

$$1.\, \Phi_F = 60mV * 6 = 0.36V$$

$$W_{max} = \sqrt{\frac{2\epsilon_{si}}{qN_a} 2\Phi_F}$$

$$2.\, C_{min} = \frac{C_{ox} C_{dep}}{C_{ox} + C_{dep}}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 * 8.85 * 10^{-14}}{10 * 10^{-7}} = 345 \frac{nF}{cm^2}$$

$$C_{dep} = \frac{\epsilon_{si}}{W_{max}}$$

$$3.\, V_T = -\frac{Q_d}{C_{ox}} + 2\Phi_F$$

$$V_{T,ideal} = 0.82V \text{ to } 1.2V$$

So, I mean in a way you know this is a sort of laziness to, refusing to calculate. But it turns out that when you force yourself you know to not calculate if you have a calculator you immediately run for it and then you churn out some numbers. But you will not be thinking that much. When you are refusing to calculate then your mind is forced to think. And then many times you come up with many interesting solutions.

So, it is a good thing that you can do. But, of course, not in the exams, exams you need to be exact. This is only for learning purposes.

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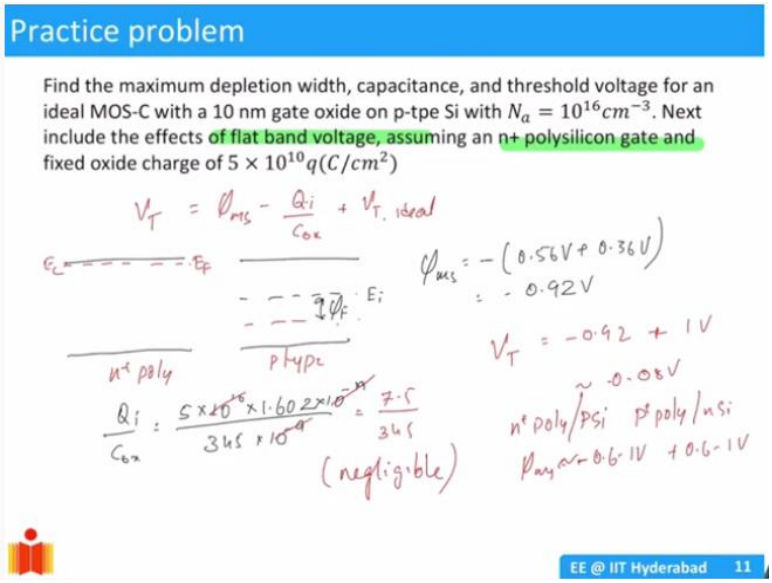

So, the last part of the question was basically calculate the flat band voltage assuming n plus polysilicon gate and fixed oxide charge.

$$V_T = \Phi_{ms} - \frac{Q_i}{C_{ox}} + V_{T,ideal}$$

$$\Phi_{ms} = -(0.56 + 0.36) = -0.92V$$

$$\frac{Q_i}{C_{ox}} = \frac{7.5}{345} \ (negligible)$$

$$V_T = -0.92 + 1 = 0.08V$$

So, this is going to be simply 0.08 volts something like that in that range. So, you see this is one advantage of actually choosing n plus poly with p-type substrate. Since you have this large phi ms which is negative for you know if you choose n you know n plus poly p silicon combination or p plus poly n silicon combination. Phi ms is going to be large negative. You know approximately minus 1 volt. You can take it.

Here, phi ms is going to be not 1 volt 0.8 to 1 volt or 0.6 to 1 volt I will say. Here, it is going to be plus 0.6 to 1 volt because in this case of p plus poly n-type silicon it is going to be phi ms is going to be larger. So, it is going to be positive number. So, what happens is when you

calculate the V_T you had this V_T ideal term which is Q_d/C_{ox} plus 2 phi F. That is going to be a large positive number for n MOS devices.

So, phi ms is going to bring it down. So, overall V_T of the device is going to be small if you use n plus poly and p type and similarly p plus poly and n type. Absolute number absolute magnitude of V_T is going to be small. And it is going to be quite symmetric. This is very useful in the newer generations where you do not want V_T to be large. We want to accurately control it.

Thank you so much. I will see you in the next lecture, bye.