Introduction to Semiconductor Devices
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Lecture - 8.2
MOSCAP Capacitance-Voltage (CV) Characteristics

Hello, everyone. Welcome back to Introduction to Semiconductor Devices. So, in the last lecture, we understood the, last few lectures we have understood the MOS capacitor electrostatics and we also looked at the various non-idealities. So, today the agenda is to understand the CV of a MOS capacitor, sorry. A CV is a very important measurement technique which will help us analyze the behavior of a MOS structure. So, we will spend some time today on that.

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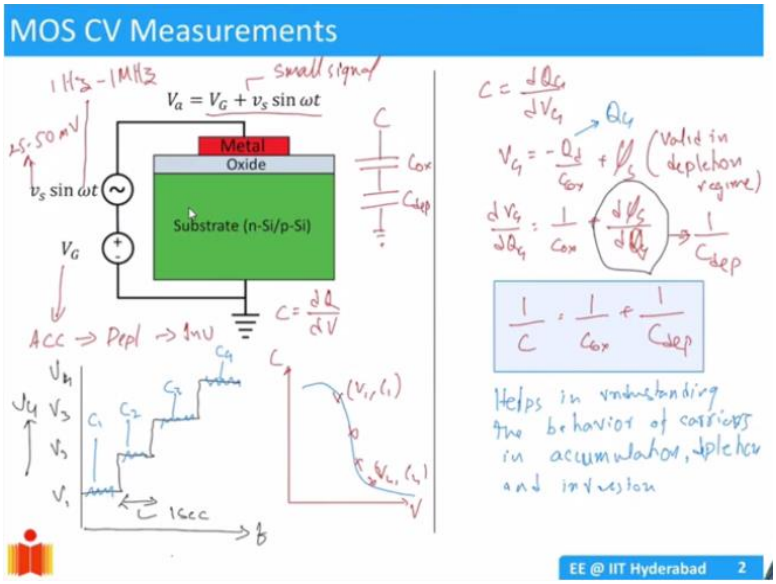

So, we have seen this already. So, wherein you have the MOS structure metal oxide and semiconductor. We have analyzed this in detail. So, essentially what we have been doing is we are drawing a band diagram and all in this direction basically from going from metal to oxide to semiconductor what was happening we understood that in multiple ways. So, today we would like to understand CV.

When you take of a CV capacitor, if you take a parallel plate capacitor, what is its capacitance? The capacitance is simply you know the capacity to store charge. Let us say you apply a positive voltage you apply a charge you know voltage to one of the plates then it develops positive charge. And there will be an opposite equal and opposite negative charge on the other plate. And there is a certain amount of energy stored in the capacitor.

The ratio of, you know charge to voltage is your capacitance. So, for a simple parallel plate capacitor, if you add a plus delta q, there will be automatically a minus delta q on the other plate. And it is a, you know constant. The capacitance is constant. But in semiconductor devices, the capacitance is not constant. We have seen one example in the case of the PN junction diode in reverse bias.

So, as you increase the reverse bias, we saw that the depletion width was increasing and the capacitance was changing. So, now we would like to understand what happens to the MOS device. So, it is not a simple PN junction. But you have an oxide in between and then the metal and the semiconductor. To understand that, what we will do is we will apply 2 voltages to the MOS structure. One is a DC voltage which I am calling as V_G.

This is basically a biasing voltage. So, I will change this from accumulation to depletion to inversion. I will sweep through these regimes. I am essentially changing the DC bias when I change my V_G. In addition to that I will apply a AC signal. So, the total AC signal is basically V_G plus some AC signal. Wherein this AC v_s is a small signal voltage you know it can be something like 25 to 50 millivolts. It is a small signal.

It is not going to perturb the DC operating point of the MOS capacitor. And then I will have another you know frequency that could be anywhere you know it could be 1 hertz to even 1 megahertz. You know it could be a wide range of frequencies. So, I am doing a, I am checking the response for small signal. v_s is small single voltage. Now, how does this structure respond? But, how do you measure capacitance?

If you want to measure capacitance, what we will do is we will essentially change. We will C is basically dQ/dV. So, I will change my AC signal. So, that is my you know frequency certain frequency I am changing that and looking at the response of the charge. And then from that I

am calculating the capacitance. In practice, the way to do this would be I will apply a voltage with respect to time.

So, let us say I have my I will sort of step voltage I will apply. So, basically I have my V_1, V_2, V_3 and V_4. So, I am stepping my DC voltage. This time duration could be like you know 1 second. It is a lot of time. It could be millisecond as well. So, as a function of time, I am changing my DC voltage. V_G is changing in this direction as a step.

In addition to DC, I have a small AC signal on this riding on this. You know in this there is a small AC signal like this. So, I will use an LCR meter that is a standard equipment to measure the capacitance. So, I will use an LCR meter and I will measure C_1 here, C_2 here, C_3 here and C_4 here. So, I am getting capacitance as a function of voltage. So, I will take this and I will plot voltage versus capacitance. So, that is what we call as a CV.

It could be some shape like this. So, it is essentially a collection of these points you know. So, collection of these points is essentially your CV curve. And that gives you a whole lot of information. What sort of information? Well, to understand that, let us go back to what the capacitance will give you.

$$C = \frac{dQ_G}{dV_G}$$

$$V_G = -\frac{Q_d}{C_{ox}} + \Phi_s \quad (valid\ only\ in\ depletion\ regime)$$

$$\frac{dQ_G}{dV_G} = \frac{1}{C_{ox}} + \frac{d\Phi_s}{dQ_G}$$

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

So, in effect, what we are seeing is you have a oxide capacitance and then you have a depletion capacitance in series. So, that seems reasonable. We saw that there is a depletion region created. So, just under the oxide there is going to be a depletion capacitance. And then there is a series relation with the gate oxide capacitance. So, you have these 2 capacitances. So, this relation you know this helps in understanding the behavior of carriers in accumulation, depletion and inversion.

So, we study this function how this is happening. So, that is the analysis CV analysis. So, how does the CV curve look like? You know we will first show you that.

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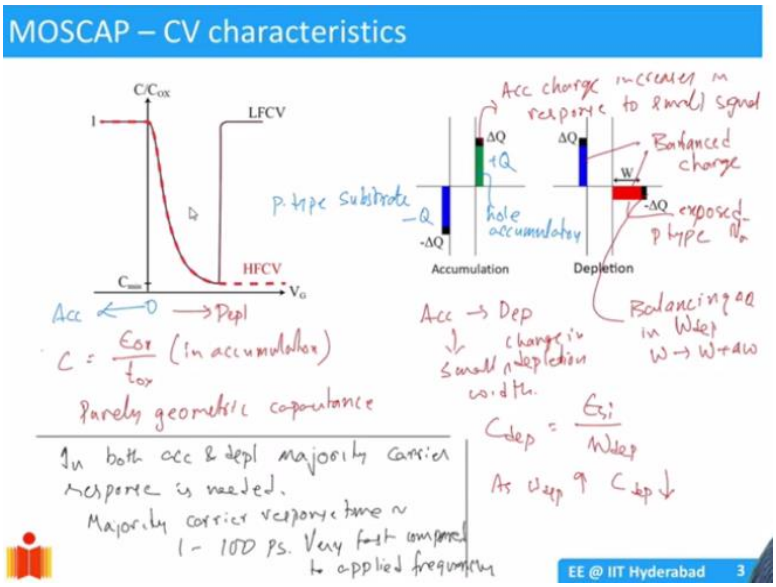

And we will explain how that is coming about. So, the CV curve looks like this. So, you have basically on the y axis C/ C_{ox}. So, I am plotting the capacitance versus C_{ox} and then x axis is the voltage. So, we will understand this in a, by region by region. So, first let us consider the accumulation region. And this is a p-type substrate. So, p-type substrate, let us just assume that for a moment.

So, how does it look like? What happens in accumulation? If you take a p-type substrate and apply a negative voltage to it you are essentially going to drive the holes. You are going to attract the holes to the interface. And because of that you have accumulation. So, that is schematically shown here. So, this is your hole accumulation. So, this happens right at the interface. And there is an opposite you know there is going to be a minus Q here.

And there is going to be plus Q here. It is always going to be valid for any capacitor structure. So, the voltage is below 0 if I call this as 0 here for example. This is my accumulation. And in accumulation, what you are seeing is if I you know this is my you know this is this plus Q and minus Q are caused by the DC voltage. V_G I am biasing the capacitor and the small signal is going to cause a small you know minus Q minus delta Q let us say.

This is a small signal contribution, this black region. So, if we have this minus Q here, minus delta Q there is going to be plus delta Q. So, you change the gate voltage by tiny amount the

balancing voltage sorry you change the gate charge by tiny amount and then the balancing charge will be in the accumulation charge in the accumulation. So, basically your Acc charge increases in response to small signal.

The small signal is not really changing the bias you know biasing condition is still accumulation. But for every small delta Q that we add on the gate, there will be a positive delta Q that will be added on the accumulation rate. So, the capacitance is like a parallel plate capacitor. You add a plus delta Q on the one plate minus delta Q will be on the other plate. So, the capacitance is going to be C accumulation, let us call it.

$$C = \frac{\epsilon_{ox}}{t_{ox}} \quad (in\ accumulation)$$

It should be epsilon oxide divided by t of the oxide thickness of the oxide. Well, this is the overall capacitance. So, even I could call it you know in the accumulation I can write it as you know I can remove this part. You can say C is equal to this in accumulation. So, in understanding the CV, we have to think about for every plus delta Q where is the minus delta Q going to come from.

The balancing charge, where is it going to come from? That will determine your capacitance. And remember, this is basically in the accumulation it is a purely geometric effect. What happens in depletion? So, we know that as you increase the gate voltage from 0 onwards it will be depletion. This will be depletion. What happens? You are going to push away the holes. This is a p-type substrate.

So, we are going to push away the holes. So, you get exposed acceptors. Expose Na minus exposed Na minus expose the acceptors. So, that is going to balance. So, basically this balanced charges. So, the electrons are the, sorry the metal has positive charge now. And that will be balanced by the negative charge created with a depletion region. Now if you add a tiny delta Q on the metal the minus delta Q is going to come from the edge of the depletion region.

Remember, we are not changing the bias. So, it is a small change. So, this is the balancing delta Q in depletion region. So, basically w is going to change from w to w plus delta w something small change in the depletion width. So, that will lead to a capacitance. So, when you go from

Acc, accumulation to depletion, small depletion width or I should say small change in depletion width.

So, this gives you what is known as depletion capacitance C depletion which is simply epsilon by the thickness of the depletion width depletion of thickness of the depletion region.

$$C_{dep} = \frac{\varepsilon_{si}}{W_{dep}}$$

So, this we have discussed when we talked about PN junctions in the reversed bias. So, even though it is very you know different from what you know parallel plate capacitor. You have parallel plate capacitor with plus Q and minus Q separated by insulator.

But in the case of a semiconductor depletion region, it is a distributed charge. Na is not like plus Q minus Q. It is a distributed charge. But we saw that overall even then the net capacitance is simply going to be epsilon by width of the depletion region. So, what happens? Well, as w depletion increases C depletion reduces. That is what we expect anyway. Depletion capacitance is reducing.

So, in both accumulation and depletion, majority carrier response is needed. In accumulation, it is simply the majority of the carriers which are holes in this case are going to accumulate. In the depletion, we are going to push away the majority carriers. So, it is still the majority carrier response.

And it turns out that majority carrier life majority carrier response time is approximately you know 1 to 100 picoseconds. It is very fast compared to the applied frequencies.

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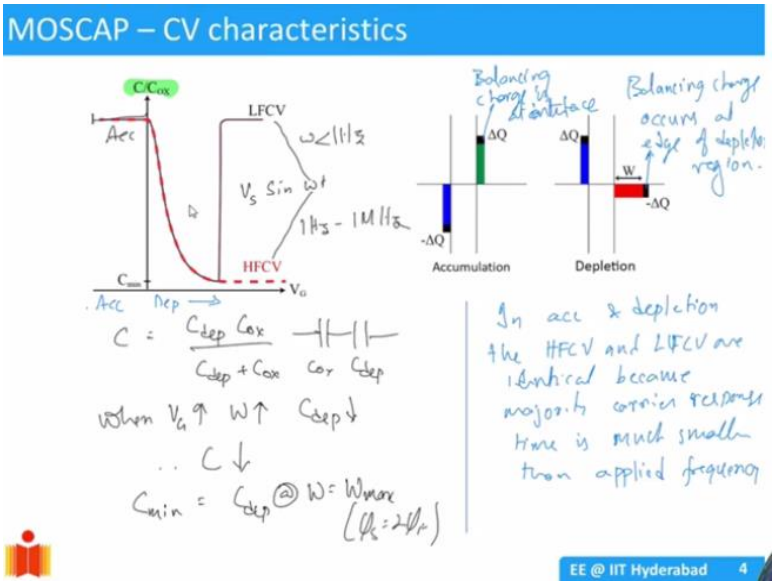

So, let us before I talk about that let me you know talk about how the CV changes. So, in accumulation, we saw that the, it is purely geometric capacitance and Cox. So, when we plot C/ Cox is going to be 1 in accumulation. When you go to depletion,

$$C = \frac{C_{dep}C_{ox}}{C_{dep} + C_{ox}}$$

Because we have 2 capacitors in series here, Cox and C depletion, you have to write this. And your C depletion is reducing. When VG increases, w increases. So, C depletion decreases. Therefore, C decreases. So, that is why as you go into depletion, there is a gradual change in the capacitance. Now, what is the minimum value? Well, the minimum C min, so, minimum value of capacitance you will get when you get the maximum depletion width.

So, C min equal to C depletion at w equal to w max. You know whatever is the maximum depletion width, w max occurs when phi s equal to 2 phi F. You have the maximum depletion width and with respect if you calculate the C depletion at that point you will get the C minimum. So, why does the majority carrier response time play a role here? We said majority carrier response time is very fast compared to the applied frequencies.

So, in CV, we tend to make a measurement set quite different frequencies you know. One of them we call as low frequency. One of them we call as high frequency. So, remember, we talked about a AC component sign AC signal small signal which has a omega term which is a frequency term. So, if this frequency term is anywhere from 1 hertz to even up to 1 megahertz we call it HFCV.

If you go below that what happens is we call this as you know LFCV. Omega less than 1 hertz, I would say. In fact, millihertz kind of range we do. We do what is called as quasi static measurement to actually capture LFCV. Experimentally, it is quite challenging to measure LFCV. HFCV is quite easy. So, you see that since majority carrier response time is fast you know it is in the order of picoseconds, you do measurements at whatever frequencies you want.

But you are going to get CV which is identical. So, the red curve is a HFCV. The black curve is a LFCV. In the accumulation and the depletion part, it is identical. This is Acc. And this is depletion to this point. So, in Acc and depletion, the HFCV and LFCV are identical because majority carrier response time is much smaller than applied frequency. It is nearly identical. But one important difference exists. That is where the balancing charge happens.

In accumulation, balancing charge is at AC in our interface at the silicon silicon dioxide interface. Whereas in depletion, there is nothing like you know there is no the possibility of you know inversion has not yet happened. Inversion requires a certain surface potential. We have not reached that. Till you reach it, you are going to simply push away the majority carriers. So, balancing charge occurs at edge of depletion region.

This is a primary difference between accumulation and depletion. Physical locations are different. But, you know this time is still much faster compared to the applied frequencies. So, of course, that tells us that in inversion it is not going to be the same.

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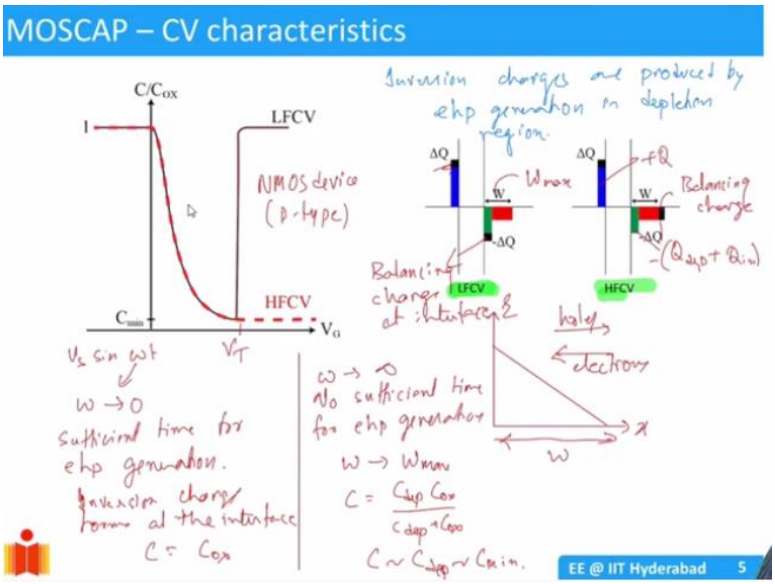

Why is it not going to be the same? Well, in inversion, charges are produced how, are produced by ehp generation in depletion region. This is how inversion charges are produced. Well, correct. So, what happens to this electron hole pairs which are produced? So, what we need to do is you look at how the electric field is. Sorry, this is let us say x versus electric field. And you know that it is going to be like this.

This is my depletion width, w. So, a linear function electric field is linear. So, what will happen to holes? Holes will go this way. And electrons will go in the opposite direction. This is how the charge separation happens. And because of that, if you are doing frequent measurement at low frequency, what do I mean by low frequency? Well, my you know vs sine omega t. It is very small milliseconds a millihertz kind of frequencies.

Let us say, omega tends to 0, very small frequency. That means I am very gradually changing my VG. Then you have a sufficient time for the minority carrier generation or you know electron hole pair generation. So, sufficient time for ehp generation. So, what happens? They get generated. And then they will accumulate at the interface. Inversion charge forms at the interface.

So, if you know you have the DC bias, DC bias is such that you have this w here which is depletion width and effective this will be w max. It will be the maximum depletion width possible in that. And then you add a plus delta Q here. So, balancing charge at interface. The reason it is forming at interface is you are doing it very slowly. Remember this is you know I am saying this is for LFCV and this is for HFCV.

In LFCV, you are doing it very slowly in such a way that there is sufficient time for the electrons to accumulate you know to come to the interface. So, that forms a balancing charge. So, your C is simply going to be Cox. And that is why if you look at the curve here LFCV curve. The black curve is LFCV and immediately goes up towards C ox once the inversion forms. So, this point I will call it this as VT threshold voltage.

So, once you hit that you have sufficient amount of inversion. And then whatever changes you do it just happens at the interface and capacitance goes back upto Cox. That is why C/C ox is going to be 1. Whereas, if you do it at high frequency HFCV, let us say omega tends to infinity.

I mean, for our purposes, even megahertz is infinity. So, if you go to high frequency, your gate voltage is changing very fast.

So, inversion charge or you know there is no sufficient time for ehp generation. So, no inversion charge, I mean there is a DC you know whatever inversion this is there still there. So, I have my plus Q here. And my minus Q is formed by do this, do of 2 of this. So, this will be formed by Q depletion plus Q inversion.

Both are you know minus both are exposed acceptors and in this case electrons. So, you have these 2 charges. Now, if I add a plus delta Q, the minus delta Q can only come from extending the depletion region. This is a balancing charge. Why this has to come at the edge of the depletion region? Because, there is no sufficient time for electron hole pair generation. So, the inversion charges cannot come to the interface.

So, but we also know that once we reach threshold there is a lot of screening because of the inversion charge. So, the depletion width does not change so much. So, w tends to be w max. So, C depletion tends to be or rather the total gate capacitance. C is basically C depletion times C oxide divided by C depletion plus C oxide. So, at maximum depletion width, C tends to be close to C depletion. We will call it as C minimum.

So, that is why you see that you know there is this HFCV which does not go back up. It remains flat. So, this is the primary difference between HFCV and LFCV.

So, fine, we get this C minimum. So, by the shape of the CV, we can analyze a lot of things about the MOS device. We will take some examples. We will also run some nanoHUB simulations to show you how the parameters will affect CV. So, so far, we have considered only n MOS device. This was n MOS device. I did not mention it.

But this is a p-type substrate. All the charge diagrams are all for a p-type substrate. What happens if you take an n-type substrate? So, to explain that, I have a, you know exercise from the textbook.

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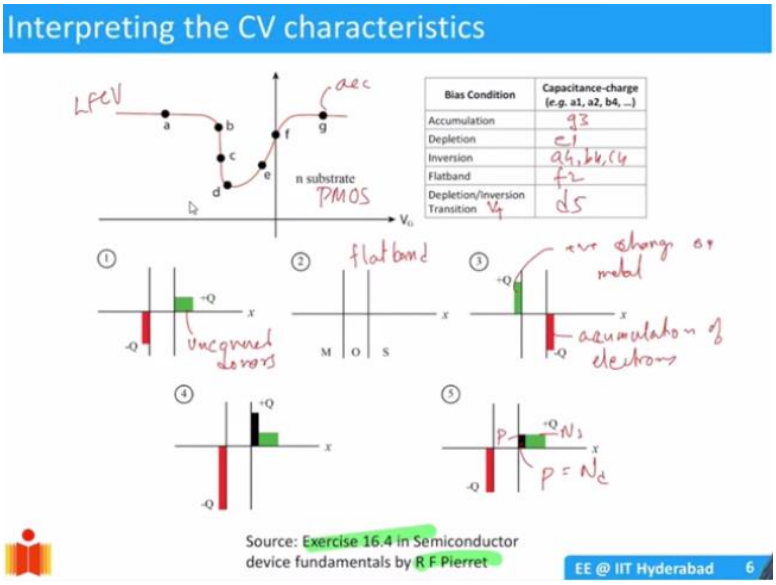

So, please go and refer to Exercise 16.4 in Pierret. This is adapted from there, so, essentially here the CV shown on the top. So, you see that there is a, you know if you have a, this is n substrate, p MOS. So, when you apply a positive voltage, what happens? You will accumulate electrons at the interface. So, you have accumulation. And as you go and apply more and more negative voltages, you will go into flat band, depletion.

And then finally, inversion and like this. This is my LFCV. This is definitely LFCV. So, we have to understand how you know each of these black points represents some kind of a physics accumulation, inversion, depletion and so on. So, we want to understand you know which point corresponds to which block charge. And in fact, you could also draw the band diagrams and look at you know which accumulation how does a band diagram look and so on so forth.

You can do a lot more you know. We can give you a whole range of exercises. We will give one of this, such things and the assignment and in the final exam there is going to be something on this for sure. So, first let us look at accumulation. This is clearly accumulation. In accumulation, what do you expect? We have excess negative charge on the substrate. So, and that has to be at the interface. This is accumulation.

So, if you look at all these examples, this is accumulation of electrons. And this is holes on the positive charge on the metal. So, both these are right at the interfaces. So, the condition g is accumulation and the block charge is 3. So, I will write this answer as g3. So, that will tell me what choice is correct. So, I have to match all of these points to the block charges. Depletion, how does the depletion look like?

Well, in depletion, there is no you are pushing a electron. So, you will have positive charge. And, where do you have positive charge which is balanced by a negative charge on the gate? So, well, there is one more point that I have to discuss here which is as you go from accumulation, as you keep increasing decreasing the voltage, at one point, you are getting to what is known as flat band. Flat band means with no applied voltage.

You know, there is, how do the bands look like? There are no bending of the bands. So, there is no charges associated with applied gate voltage is 0. So, this is my, this, the second picture is called as flat band. So, I will call this as f2. This is flat band condition without any voltage. When I apply a negative voltage, I am depleting. And so, depletion is going to be e, point e. And the corresponding charge diagram is going to be we said depletion.

We are uncovering the donors. So, this is how this is uncovered donors. So, this is going to be e1 and d is basically the threshold at the threshold at which your, the electron charge, or you know we are taking n-type substrates. So, hole charge inversion charge number of holes p is equal to Nd. Donor charge in the substrate. See here, this is Nd and this is the number of holes. So, they are equal.

That is the onset of inversion, so, threshold. So, this is called as depletion to inversion transition or V_T you know threshold. So, this is going to be d5. And the rest of them, a, b, c, semiconductor is already in the inversion here. So, when you have inversion essentially you have plus Q and there is a large sorry minus Q. And there is a large plus Q here. So, all of these points are that. So, I could write simply a4, b4, c4.

So, telling you that it is just inversion everywhere. You know all this. You cannot distinguish from a qualitative picture. a, b, c as a is going to have more inversion charge but it is very difficult to distinguish that in a qualitative way in this sort of way I think. So, but you know this sort of gives you the overall picture of how a CV looks like. So, please take your time. Review this video one more time. And see how you know you can understand.

And then we will also discuss you know how the CV changes with some parameters. So, I will see you in the next class next video. Thank you so much. Have a good day.