Introduction to Semiconductor Devices
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Lecture – 7.5
Threshold Voltage in a MOSCAP

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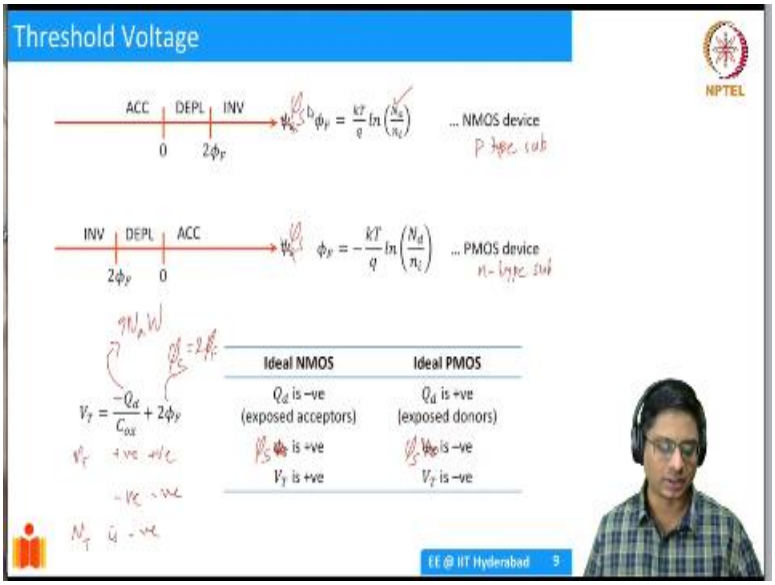

Let us get started where we left off. So, we want to define threshold voltage and this is a very important thing, because this is what you will use in the problems and in the MOSFET also threshold voltage plays a very, very important role. So, what is threshold voltage? So, we have defined, what is threshold? We said that threshold is that voltage at which surface inversion charge is equal to the bulk doping.

So, we will consider NMOS device and PMOS devices. In NMOS device, we said if the doping density was let us say N_a. NMOS device means it is a p type substrate. Correct?

$$\phi_F = \frac{kT}{q} ln\left(\frac{N_a}{n_i}\right) \quad \ldots . NMOS\ device$$

$$\phi_F = -\frac{kT}{q} ln\left(\frac{N_d}{n_i}\right) \quad \ldots . PMOS\ device$$

So, just an axis of surface potential. Whenever, your surface potential was less than 0, it was accumulation for NMOS device, because that will accumulate holes in the interface and between 0 to 2 phi F, It was called depletion. We are pushing away the holes but once we cross 2 phi F, it is inversion because we are creating electrons at the interface. So, this was NMOS device which you have seen in detail. The exact opposite thing happens with PMOS device.

Whenever your surface potential is greater than 0, it is accumulation. Why? Because it is an n type substrate, we apply a positive voltage, positive surface potential, you will accumulate holes. So, that is why it is accumulation and once you go surface potential goes from 0 to 2 phi F, it is depletion and if you increase beyond 2 phi F, call it inversion. So, for example if I take my N_d to be 10^{15}, phi F is going to be 5 times 66.3 volts.

So, if your surface potential is greater than – 0.6, that means – 0.7, – 0. 8 and so on, it will be inversion. So, this is a simple way of remembering this and we have also defined what is threshold voltage.

$$V_T = -\frac{Q_d}{C_{ox}} + 2\phi_F$$

$$Q_d = qN_aW$$

We will calculate that. One important point, I want you to note is in our definition of V_T here. This is the definition of V_T.

Ideal NMOS:

Q_d is -ve (exposed acceptors), ϕ_s is +ve, V_T is +ve

Ideal PMOS:

Q_d is +ve (exposed donors), ϕ_s is -ve, V_T is -ve

So, I want you to note this complementarity. It is very important for us later on. In CMOS, this is very, very essential. This complementarity into voltages so, fine. Let us try to solve some problems.

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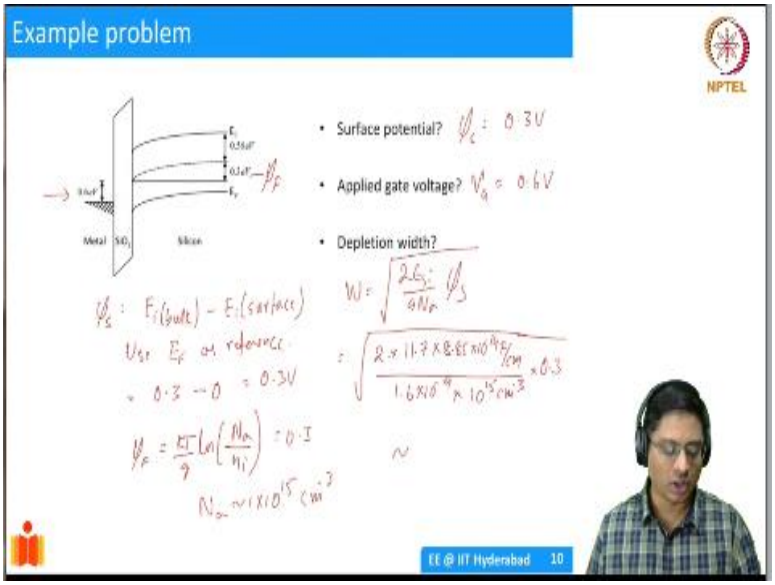

Let us look at this band diagram. And let us calculate what is its surface potential, applied gate voltage, depletion width?

$$\phi_s = E_{i(bulk)} - E_{i(surface)} = 0.3 - 0 = 0.3\ V$$

Do it for inversion also; do it for accumulation by yourself. What is the applied gate voltage when you look at this particular band diagram?

Well, the gate voltage is simply the displacement of E_F in the semiconductor and with respect to the semiconductor, what is the displacement of E_F in the metal? So, metal work function has been pulled on here and this is E_F in the semiconductor, the distance is 0.6. So, the applied gate voltage V_G must be 0.6 volts; just show the band diagram we assumed. What is the depletion width?

Well, this could be tricky. How do you calculate the depletion width? Well, we know the depletion width formula.

$$\phi_F = \frac{kT}{q} ln\left(\frac{N_a}{n_i}\right) = 0.3$$

$$N_a = 10^{15}\ cm^{-3}$$

$$W = \sqrt{\frac{2\epsilon_{si}}{qN_A}\phi_s} = \sqrt{\frac{2 * 11.7 * 8.85 * 10^{-14} * 0.3}{1.6 * 10^{-19} * 10^{15}}}$$

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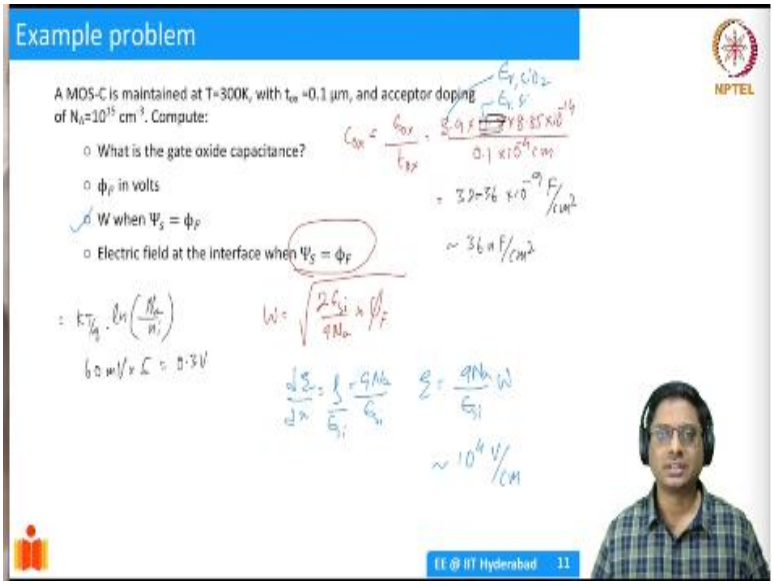

Another problem a MOS capacitor is maintained at T =300 K, t_{ox}=0.1μm and acceptor doping is 10^{15} cm^{-3}. Compute the gate oxide capacitance. What is the gate oxide capacitance? ϕ_F in volts? W when $\psi_{s=}$ ϕ_F? Electric field at the interface when $\psi_{s=}$ ϕ_F?

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 * 8.85 * 10^{-14}}{0.1 * 10^{-4}} = 36 \frac{nF}{cm^2}$$

$$\phi_F = \frac{kT}{q} ln\left(\frac{N_a}{n_i}\right) = 60mV * 5 = 0.3\ V$$

$$W = \sqrt{\frac{2\epsilon_{si}}{qN_A}\phi_F}$$

$$E = \frac{qN_aW}{\epsilon_{si}} = 10^4\ {}^{V}/_{cm}$$

So, please make sure that you do that. So, this is how you solve a few problems. So, I know, I have spent a lot of time explaining the concepts this week. But those are essential to understand MOSFET in depth.

You might be wondering why do you want to have so much deep understanding. Well, the reason is right now, we are in 7 nanometre technology. And we are actually going even smaller than that. The technology is evolving very fast. And our syllabus also has to evolve like that.

We should not be happy solving you know formula based questions. We need to develop a deeper insight. So, that we understand the state of that.

So, that is why we are introducing a lot of concepts into this curriculum. So, I wish you good luck, please take your time, review all this videos. I will also quickly record another video wherein I will show you Nanohub. How to use Nanohub? How to analyse some of this MOS capacitance? So, it will be interesting, I am sure just take your time, try it out. We will give a couple of assignment problems based on running the Nanohub tool.

So, once you do that, you will be all set. In the next week, we will discuss more about capacitances what happens you know, some of the effects will be discussed. So, I will meet you there. Thank you so much. Bye.