Introduction to Semiconductor Devices
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Lecture – 7.3
NMOSCAP in Inversion Mode

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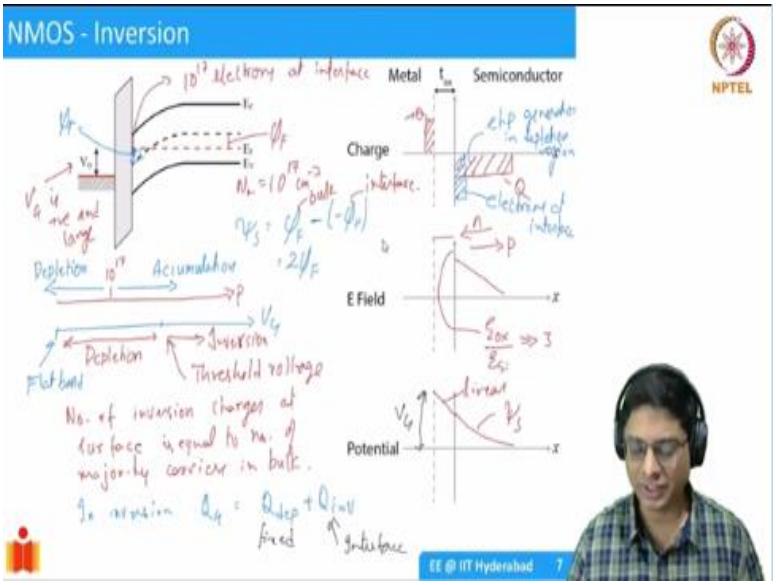

Welcome back. So, now, we would like to look at NMOS device in inversion. So, I am not really going through the motions of drawing the band diagram. I am simply showing you but by now, I think, we should be familiar. So, whenever if we want to get inversion, we need to apply positive gate voltage. So, V_G is positive and large actually, it is not simple. We are actually going beyond inversion.

We will discuss that in a moment and large and because of that, you have, first, we have depletion of the semiconductor and then we have inversion. So, what happens? You know, to understand this, let us try to first look at the, you know bulk region. Let us say, we have here, there is ϕ_F. Let us say, this is basically $N_A = 10^{17}$. Let us take this as an example, centimetre cube.

So, now, if you change your concentration at the surface, so I will say the hole concentration, so basically, if you have the hole concentration, if this is p and I have my 10^{17} at equilibrium, So, if I go here, if I increase my hole concentration, I am calling this as accumulation and when I go lower than this, I am calling depletion.

So, once I cross my once my E_F at the surface, this is E_F at the surface, if it crosses my E_i, essentially the hole concentration is less than the intrinsic hole concentration. So, what you have now is basically the Fermi level is closer to E_C. So, because of that, you have holes and as we keep increasing the gate voltage, suppose in this case, let us say I increase, this is my gate voltage axis V_G, initial is 0, I will be at flat band.

This is 0 flat band and then as I increase V_G, I will first to reach depletion. This will be the depletion region and after depletion at some point, we are going to get into what is known as inversion, this, which is called as threshold voltage. What is this threshold voltage? To analyse that, first, we will look at the surface potential. So, the way, we define threshold is, in the case of an NMOS device or other, the number of inversion charges at surface is equal to number of majority carriers in bulk which mean that let us say, in this case, 10^{17} is the number of holes in the bulk.

Then we need to have 10^{17} electrons at the interface. So, here, 10^{17} electrons at interface. How do you know that? Well, I mean have carefully drawn this in such a way that this is my ϕ_F and even this is going to be my ϕ_F. The distance is ϕ_F again. So, now, what is the surface potential here?

$$\psi_S = 2\phi_F$$

So, in the bulk, it is ϕ_F minus in the surface it is actually $-\phi_F$, minus of $-\phi_F$ equal to 2 ϕ_F. This is bulk. This is interface. So, basically whenever surface potential reaches to ϕ_F, we say that there is inversion. We still have to relate surface potential to the gate voltage. We will do that in a moment. Before I go into that, I want to discuss the way the charges look like.

So, what happens is; we are applying positive voltage so, there is going to be a positive charge on this side + Q. And then what happens to the semiconductor? We have depleted it. So, there is going to be some depletion charge – Q. But as we increase the depletion, there is electron

hole pair generation in the depletion region. So, this is EHP generation in depletion region. This becomes significant after point.

If there is EHP generation where will the charge go, well, we will again redraw this just before the inversion is reached, let us say. What is the electric field? The electric field is going to be this and this. This is just before electric inversion, but once you reach inversion, essentially what we are saying is; I mean, let us say, we cross the inversion. We have electron hole pair generated.

Electrons will come in this direction. Electrons will move here. N will go this direction. Holes will go into the bulk. This electric field is in the +x direction. So, what happens is whenever inversion is reached, you are going to have an additional charge at the interface. This is electrons at interface. Total now, once inversion is reached.

So, at inversion, for any inversion, Q_G = Q depletion + Q inversion. So, in the semiconductor, there are 2 types of charges. One is the depletion charge which is fixed. But electron hole pairs that are generated are free to move about. So, electrons will come towards the interface. Just at the interface, it is a very, very thin layer of depletion inversion charge.

And because of that, this discontinuity will actually increase. If you look at, this will give you this as an exercise. So, look at this, if you look at E_{OX}/E_{SI}, this will be greater than 3, much, much greater than 3 in inversion.

If you have inversion charge, this is how it will behave. So, the inversion charge also is at the interface. You should not forget if you remember that and then the hole, anyway, will go to the bulk. How will the potential look like? If you are right at inversion, the potential is going to be simply again the same quadratic behaviour. This is ψ_s. And then there is a linear relation. The total is my V_G.

So, the voltage still falls always across the 2 oxide in the semiconductor. So, this will help us actually derive what is the relation between the gate voltage and the chi. Remember, we said at threshold, $\psi_s = 2\phi_F$ that is something that we can easily compute.

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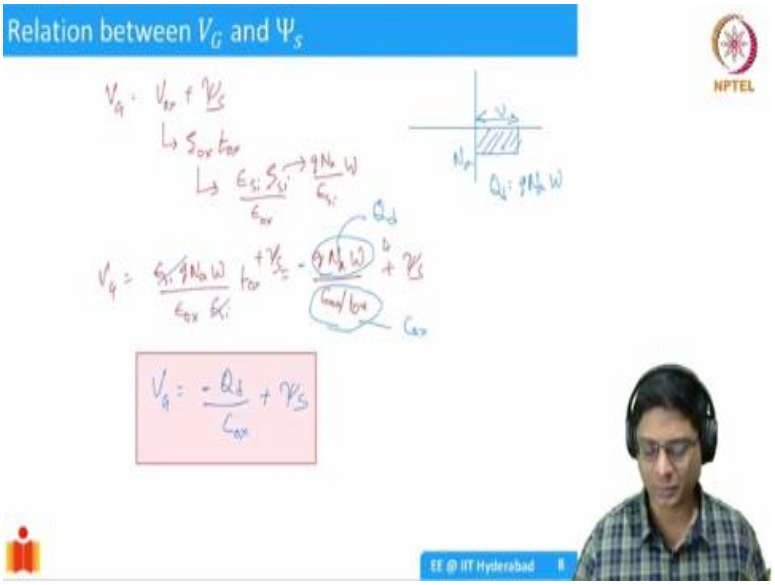

$$V_G = \frac{qN_AW}{\epsilon_{ox}/t_{ox}} + \psi_s$$

$$Q_d = qN_AW$$

$$V_G = \frac{-Q_d}{C_{ox}} + \psi_s$$

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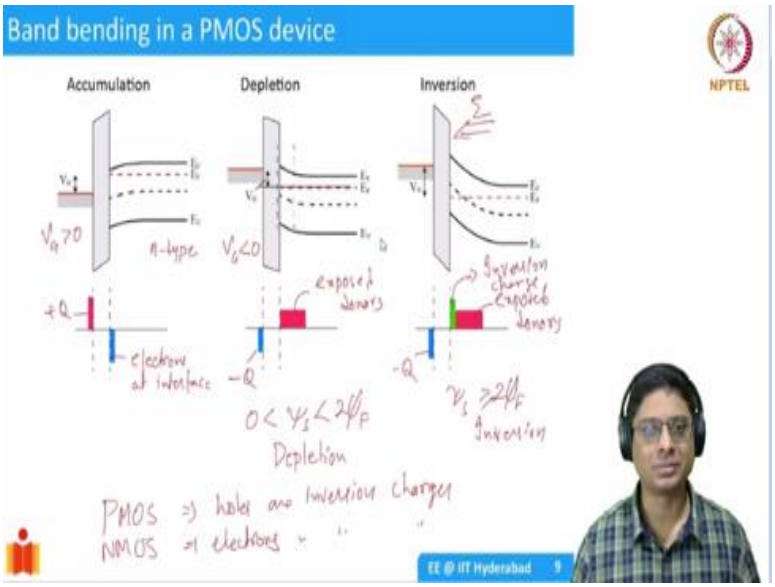

So far, we have discussed only the NMOS device. So, we have taken a p type substrate, but in a PMOS device, we have to take an n type substrate. You take an n type substrate and then

apply a positive voltage, then you will have accumulation V_G greater than 0. You have accumulation.

So, any accumulation when you have no positive voltage, you have electrons accumulating at the interface that is what we are showing here. This is electrons at interface.

It is going to be the exact opposite of whatever we saw in the NMOS case in PMOS. This is + Q gate charge. Now, if you deplete, you will have these exposed donors and – Q in your gate voltage. So, we have to apply V_G of less than 0 for a PMOS device. In NMOS device, we applied greater than 0. In PMOS, we have to apply less than 0 so, that we are depleting. We are pushing the electrons away from the interface.

And then you continue increasing your so, gate voltage, you will reach inversion. So, basically one of the ways of representing depletion is basically when your surface potential is between 0 and 2 ϕ_F. This will call it as depletion. The surface potential is greater than or equal to 2 ϕ_F, we call it inversion. So, in this picture, I am representing just slightly above inversion.

So, in this case, what happens is you have these exposed donors, which are contributing the positive charge. This is your – Q anyway and you have an additional inversion charge at interface. How is this coming to the interface? Well, you have this depletion region which has been you know out of equilibrium. We removed all the majority carriers. So, then the semiconductor tries to come back to equilibrium by generating electron hole pairs.

When these electron hole pairs are generated, because the field is in the negative direction; this is a directional field here. Holes will come towards the interface and electrons will go into the bulk. So, that is why you have these holes and that is why we call it a PMOS device. So, PMOS device implies holes are inversion charges. NMOS device implies electrons are inversion charges.

That is why whenever we want to talk of PMOS device, we take an n type substrate and invert it. That means we convert n type, you know, we should have ideal electrons there, but then we deplete it and then we make it have holes. We are switching. We are inverting the semiconductor that is why we have holes as inversion charges. And this is in a PMOS device. NMOS device, electrons will be the inversion charges.

So, that is why we start with the p type substrate. So, I hope this you know, is clear to you. This is not a simple thing. I mean, this is something that, you know, I remember when I first learnt it, it looked like I learned it, I understood, but then when I look at it after a couple of years, I realised that I have not fully understood it, it takes some time for you to understand. So, please go through it a couple of times, understand the physical mechanism.

So, all these diagrams might look like you know, a lot of shapes, lots of variations. But they are all very simple to draw. If you go towards it in a logical way that has been using you know, this go step by step and all of this will be clear. And we will also relax certain assumptions that we made for an ideal MOS capacity. And so, we will do that in the next class. Thank you so much for your attention and I will see you in the next lecture. Bye.