Introduction to Semiconductor Devices
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Lecture - 7.1
NMOSCAP in Accumulation Mode

Hello, welcome back to Introduction to Semiconductor Devices. We are now in 7th week of the course. So, we are more than halfway through what we wanted to cover. And in the last week, we were discussing the operation of MOS capacitors. We looked at the depletion inversion and accumulation regimes and we understood them based on simplified band diagrams. We just looked at the semiconductor part of it.

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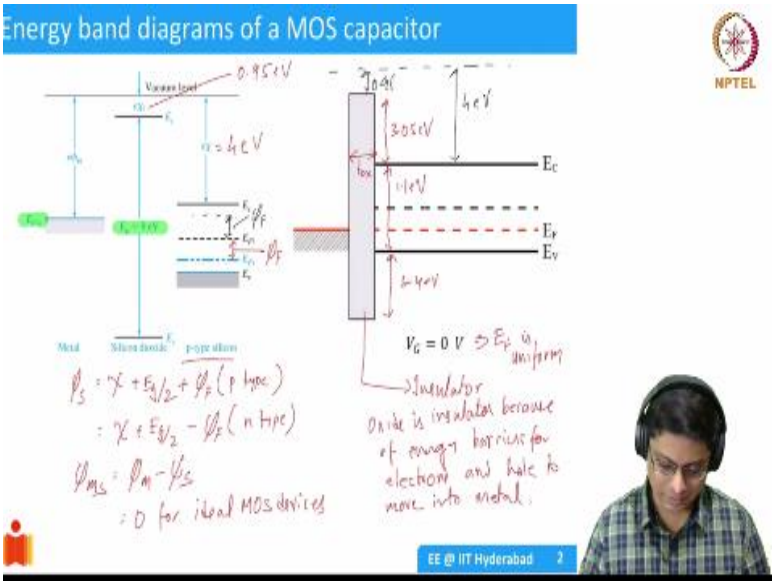

So, today, we would like to go deeper into understanding the electrostatics of MOS capacitor. And to do that, let us start with the basic bands. So, this, we have done even for the metal semiconductor junctions. So, we have semiconductor, which is having the E_C and E_V, the conduction valence bands and then there is a certain Fermi energy and we have seen already that the electron affinity of silicon.

In this case, I think about 4 eV, 4.01 eV. So, 4 eV, let stick it with that. And you know, the electron affinity is essentially the energy difference from the conduction band edge to the vacuum level. We have seen this definition before and this is a p type silicon and now, we also have an oxide in between, in between the metal and the semiconductor, we have an oxide and we know that oxide has a large band gap of you know, 9 eV.

This is silicon dioxide so, 9 eV of band gap and then it also has an electron affinity which is shown here. The distance of the E_C from the vacuum level, in this case, for silicon dioxide, it turns out to be 0.95 eV. So, it is actually electron affinity is quite small, then we have the metal which has its own Fermi energy E_{Fm}. So, we can define the work function of semiconductor ϕ_s.

If it is a p type semiconductor, you could easily define it as simply the, you know, it is essentially the distance between the Fermi energy to the vacuum level. So, for a p type semiconductor, it is going to be simply the electron affinity plus E_g by 2 and I will call this distance of Fermi energy from intrinsic levels ϕ_f. So, this distance so, basically this is for a p type semiconductor.

$$\phi_s = \chi + {}^{E_g}/_{2} + \phi_f (for\ p - type)$$

If it was an n type semiconductor, if you are using that was a PMOS device if you are using, this would be

$$\phi_s = \chi + {}^{E_g}/_{2} - \phi_f (for\ n - type)$$

for an n type, because for an n type semiconductor, the Fermi energy would be somewhere here and this would be your ϕ_f, so + E_g by $2\phi_f$ would give you the work function of the semiconductor. So, there is a; you know, right now, we are not really considered that they are in contact with.

We are still looking at all this metal semiconductors silicon oxide slightly far apart. So, we can define an important parameter which we call us $\phi_{ms}(\phi_m\text{-}\phi_s)$ which is essentially the work function of metal minus work function of semiconductor. So, this is work ϕ_{ms} and this is an important quality that we need to look at you know, when we talk of thresholds milli volt per second.

But, in our previous lectures, we have looked at an assumption, we said that for an ideal MOS capacitor, the ϕ_m is equal to ϕ_s. The work functions are same for metal and semiconductor. So, this is equal to 0 for ideal MOS devices. But you know, you will almost never have an ideal scenario because you see ϕ_s is dependent on doping. So, this has a, this one, the work function of a semiconductor is dependent on the doping density.

And you will have different varying amounts of doping and because of that ϕ_{ms} is going vary even if you just take the exact same metal. So, it is never going to be 0 for all the devices. It is going to be some number. But right now, we do not want to worry about it. We want to simplify our analysis. So, for today, we will assume that ϕ_{ms} is 0. Now, if ϕ_{ms} is 0 and you do not apply voltage, what happens when you bring them in contact?

When we bring them in contact essentially, the first thing, we have to do is draw equilibrium formula, which is a straight line. Since there is no applied voltage implies E_F is uniformly. A applied voltage is 0 implies E_F is uniform. That was the first step in drawing band diagrams, all the time. Once you do that, you draw the E_C and E_V at appropriate distances so, one important thing to make sure is the distance of you know, the electron affinity is basically given, known.

So, basically, this is 4 eV if I put a vacuum level here. So, this is 4 eV, and this is 0.95. So, basically, this particular barrier here is going to be 3.05 eV. And this is energy band gap. This is 1.1 eV. Just please remember, these diagrams are not drawn to scale. If I were to draw to scale, then this region has to be 1.1. So, this has to be 3 times this. So, I am not drawing to the scale.

Just indicated these number distances but you need to remember that this barrier is 3 times almost you know, slightly less than 3 times the energy band gap. So, it is quite large barrier. Similarly on the lower side, we have a barrier. So, this will be you know, roughly something a number between 3 to 4 eV; some number between that. Depending on the band gap, you can calculate.

So, what does this mean? Well, this is an insulator. We know that silicon oxide is an insulator, and we see that if there are let us say, electrons in the conduction band of silicon, they see a 3 eV energy barrier which is a very substantial amount of energy barrier that is why electrons

cannot go into the metal. That is why it behaves as an insulator. Similarly, if you have holes in the valence band, they too see an energy barrier of about you know, 3 to 3.5 or so eV.

So, they also cannot go into the metal or other, electrons cannot come in here. So, because of that, oxide acts as an insulator, because of energy barriers; oxide is insulator because of energy barriers in E_C, for energy barriers I would say, for electrons and holes to move into metal. And we have briefly mentioned the problem of energy barrier.

So, wherein you have a barrier like this, the height of the barrier we know, 3 eV in this case and the width of the barrier will be the thickness of the oxide. So, because of that, you can analyse and see what happens and if the thickness is large you know, if it is 10 nanometres, it is almost like a perfect insulator, but the moment that thickness reduces, this MOS capacitor starts having leakage because electrons will tunnel across the barrier.

The tunnelling current becomes significant that is the reason why the leakage current increases. In the MOS capacity, MOS device does not work as a proper capacity because of the leakage. So, this is the basic background.

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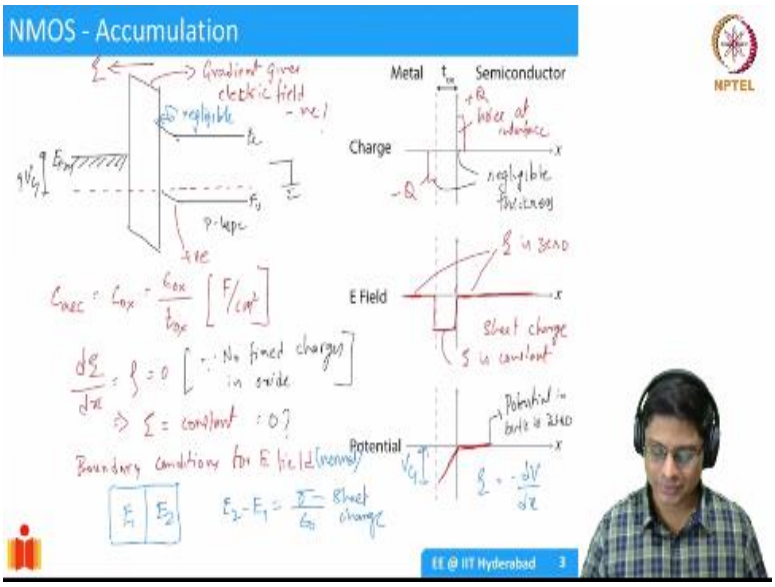

So, let us try to analyse what happens when you have a MOS device in accumulation. Let us start with NMOS device. That means I will start with a PMOS p type substrate. So, let me draw the E_C, E_V. This is my E_V. This is my E_C and it is NMOS device. So, anyway I draw the Fermi energy just for reference, equilibrium Fermi energy, there is no applied voltage. It will be like this. So, you have a p type device.

But basically, we are saying that we want to study how the NMOS device works in accumulation. And if you want to accumulate it, what is the type of voltage we need to apply? So, this is a p type substrate which has holes, and we want to increase the number of holes. So, we want to bring more holes near the interface that means you have to apply a negative voltage.

If you have to apply negative voltage, what do we do? The Fermi energy shifts up whenever you apply. So, essentially, we are applying a voltage with respect to the bulk. Let us say this bulk is you know, this is grounded and you have a metal here on the side and we will apply the voltage. I will just show that so, let us say, this is my E_{Fm}. And this is my applied gate voltage q times V_G.

If the applied gate voltage is negative, the Fermi energy moves up relative to the bulk Fermi energy. And that is why you see this. And what happens to the bands? Well, the bands we know that there is more of holes in the interface. So, we will put them like this. And what will happen to the oxide bands? The oxide band gap has to still remain you know, 9 eV. So, what we will do is what type of field should be there in the oxide.

All the way, all the time, we have to think about you know, how the field should be that will simplify our analysis. So, now you have positive charge. Here, you have positive charge. Holes have accumulated. On the other side, you have to have negative essentially putting a negative bias. So, there will be electrons on the side. So, basically your electric field is in this direction from right to left.

And so, because of that, my oxide band will bend this way. Just to indicate that this is essentially showing the gradient. Gradient gives the electric field. And in this case, it is negative. Remember why it is negative. So, this is a band diagram for a NMOS device in accumulation. So, to understand these devices, well, now we will try to draw what was called as block diagrams, block charge field and potential diagrams.

So, essentially, what we can do is here, we know that there is a positive accumulation, positive charge at the interface. So, I will represent this by putting a small block here. This is holes accumulated at the interface. Why holes accumulated at the interface? Let us say, if this is I am

sorry, I should actually make it positive. There is a positive charge so, I will draw. This is holes at interface. This is +Q charge.

So, since, it is a capacitor, there has to be equivalent opposite charge on the metal plate. So, that also will be at the interface -Q charge. So, what is the thickness of these charges? This is you know, if I took a look at these 2 charges, what is the thickness? Well, these are like infinite small sheets basically. So, negligible thickness. Why should they be negligible?

Just at the interfaces you know, but the interface between silicon dioxide and metal, we have a negative charge. At the interface between silicon oxide and silicon, we have the positive charge. Why should they be negligible thickness? Well, I mean you know, we know that the electric field inside the metal cannot be nonzero. It is 0. The thickness of the metal is such that the potential is same everywhere. And then the electric field has to be 0.

So, if I draw the electric field, I know that this is here 0. And even in the silicon, it is 0, because it is a you know, lots of holes and they behave like effectively like a pseudo metal. The semiconductor behaves like a metal. Almost like a metal. there is going to be small electric field, but we can neglect that. So, basically electric field E is 0 here in both these locations.

Remember if there was an electric field, the charges will reorient because they are all free charges; holes in the p type semiconductor and the electrons in the metal, they are free charges they can reorient in such a way that the electric field is hit. So, they cannot be any electric field in the bulk of a metal. So, that is why our charge exists only at the interface.

So, even though, I am sure by showing this you know, blocks to be a finite thickness that is only a visual way of representing it, but it is understood that they are very, very, at the right at the interface. So, you have equivalent opposite charges. So, they should be capacitors. What is the capacitance? So, the capacitance, you can think of, C accumulation, C acc, C accumulation should be equal to simply the, you know, you have the oxide and essentially the oxide capacitance.

$$C_{acc} = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}\left(\frac{F}{cm^2}\right)$$

So, we will take a C oxide because if you have you know charge + Q and – Q separated by distance, we know the capacitance already, it is simply going to be epsilon oxide divided by the thickness of the oxide and by the way, remember that this is ferrites per centimetre square. We are always dealing with the per unit area capacitances. So, we have the capacitance, and we have the field in the metal and the semiconductor. What is the field in the oxide?

Well, whenever we know, we have mastered this recipe, whenever we want to find a field, we need to solve the Gauss law. So, dE by dx should be equal to ρ but in the bulk of the oxide, there are no charges because you know, in between, you know the thickness here in this region, there are no charges. We have made that assumption when we are, when we are talked about ideal MOS capacitor so, we said, there are no fixed charges.

This is because no fixed charges in oxide, inside oxide, there is nothing. So, that means E has to be constant. Will it be 0? The outside is 0; will it be zero? Well, it cannot be 0. The reason is we know that there is a positive and negative charge and always we mentioned that there is a sheet charge here. This is a sheet charge.

So, whenever you have a sheet charge or charge discontinuity, we know, the boundary condition tells you that if you have 2 sides, need to, this is boundary conditions for E field, normal component, of course here. So, if I have 2 regions, E1, E2 and I am looking at the normal component, just a normal component only I want to look at. If I have this scenario, what is the relation between E1 and E2? Well, you know that into E1 should be equal to sigma by epsilon 0.

$$E_2 - E_1 = \frac{\sigma}{\varepsilon_0}$$

So, if we can prove this based on Gauss law, Gauss theorem, you will take a Gaussian pill box and then look at how the electric field is so, only on the top and the bottom faces of the cylinder, you can have nonzero contribution of flux. So, that will give you this. So, essentially, you discontinued in the electric field is sheet charges. So, because of that, E filed cannot be 0 in the oxide, but it has to be constant, and we know that constant has to be you know, just by looking at this picture, we know that electric field is actually going from right to left.

So, we will take you to a negative number and there is this bit here. And then show that electric field is essentially going to something like this. Here, if this is constant. So, this is how electricity looks like in a MOS capacitor. Now, we would also like to analyse what is the potential. And whenever we want to take potential, we take some reference. So, let us take the potential in bulk is 0.

Let us take this as a reference bulk, we keep it 0 and we see what happens. And there is no electric field in the silicon so, potential is going to be constant, but when you come to the oxide, there is a constant electric field so, there should be a linear potential and considering that it is a negative field, it should be like this. Therefore, what essentially, we are seeing in this diagram is that this voltage is V_G.

Whatever gate voltage you apply that voltage, negative voltage we applied that is why you are showing it in the negative axis here. This is correct. Gradient is positive but minus of that so, correct. So, we are applying a negative voltage and then that voltage is dropping across oxide and by the time, you reach the interface between semiconductor and silicon dioxide, it is falling to 0. So, we can easily know, we know the relation E is equal to – dV by dx. So, in this case, gradient is positive, so electric field is negative so, it is consistent. So, this is how your device works. This is the electrostatics of the device.

And the reason, I am taking this time to do it in depth is; you should be comfortable with this process thinking. Once you are clear about what is happening, the way to analyse MOS devices, you will see that the physics is quite simple. The band diagrams become very, very simple. So, because you see the moment, you see a band diagram like this, you know that electric field is constant, and it is negative.

Here also, it is constant. I mean, well actually, I am sure this is very, very small region, this is not going to be; this is you know it is, it seems like it is some kind of negative field, but the distance is very small. This distance is going to negligible, I am just amplifying it. And then metal is here. So, this is how NMOS device works in accumulation. So, please take your time, work through it. Make sure that you are comfortable with this. In the next video, we will talk about NMOS device depletion. I will see you then. Thank you so much.