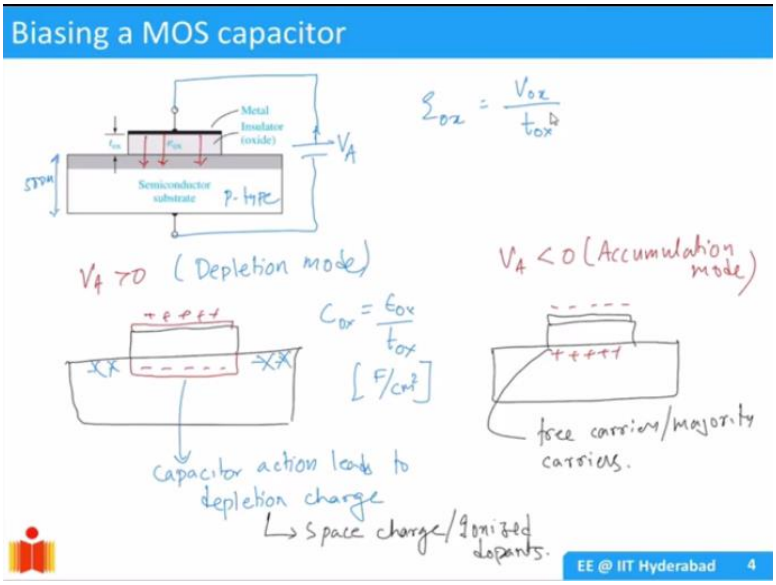
Introduction to Semiconductor Devices
Dr Naresh Kumar Emani
Department of Electrical Engineering
Indian Institute of Technology – Hyderabad

Lecture - 6.5
Operating Regimes of a MOSCAP

This document is intended to accompany the lecture videos of the course "Introduction to Semiconductor Devices" offered by Dr. Naresh Emani on the NPTEL platform. It has been our effort to remove ambiguities and make the document readable. However, there may be some inadvertent errors. The reader is advised to refer to the original lecture video if he/she needs any clarification.

(Refer Slide Time: 00:13)



Welcome back. So, we were talking about mos capacitors. We understood, what is a physical structure of a mos capacitor? Now, let us see, what happens when you apply voltage to a mos capacitor? For that I will take this mos capacitor and let us say I connect it to a battery. I will apply some voltage. Let us call it V_A, V applied. So, what happens in this case? So, remember the semiconductor is you know having certain doping.

Let us say we assume for a moment that it is P type doped. Semiconductor is P type. So, what happens? So, this is a 500-micrometre thick plate. I mean thick wafer. And we have made contact. You know we made good ohmic contact with the semiconductor. So, there is no voltage drop across that. And then there is this oxide which is t_{ox}. And then you applied a positive voltage on the other side. What do you expect?

The moment you apply a voltage across a capacitor, there is an electric field which is developed. What is the electric field? The electric field developed will be let me call it E oxide. E oxide will be simply V_{ox} divided by t_{ox}. Whatever is a voltage shock across the oxide and then there is a t_{ox}. But you know it really depends whether there is a voltage drop across the semiconductor.

Right now, let us assume that you know it is small. It turns out that it is not true but we will get back to it. So, essentially whatever is the voltage drop across the oxide divided by the thickness of oxide should give you the electric field across the oxide. So, what happens if you have an electric field? What is the direction of the electric field? Well, it is pointing downwards in this picture.

The reason is the positive terminal is on the, we are assuming that the voltage is positive we so apply positive voltage is applied to the top at the metal. And let us say the substrate is grounded. So, what should happen? So, when you have an electric field in this direction, the semiconductor is P type. It has lot of holes. And, what happens to holes when you apply a voltage like this? They will be driven away from the interface.

So, what happens is in this scenario you are essentially it looks like you know if you apply V_A greater than 0, what should happen is you will have the oxide and then you are applying metal. You know I cannot show you the metal but let us say here. There is a metal here. So, essentially it looks like you are putting the positive charge on this. And you are driving the holes away.

So, when you drive the holes away, you are going to get a region where there are no holes. And then, what if there are no holes what should remain there? Well, you know doping. It is acceptor doping. When you drive the holes away which are the positive charges which are going away then you will end up getting negative charge. And that is how you are having the capacitor action. And where is this negative charge formed?

The negative charge is only formed under the gate. You will not have any negative charge here. This is not possible. You only have because there is no applied voltage on top of it. There is no capacitor action. The capacitor action only happens under the gate. This formation of negative charge I would say is capacitor action. And how is this formed? Where is this charge exactly?

It is actually distributed because it is a uniformly doped semiconductor. The charge is distributed across, under the, you know depends on how much voltage you apply. Let us say if your capacitance is you know we can calculate the capacitance. In this case C. By the way, whenever we talk of capacitance in semiconductors, we talk of capacitance per unit area. And that will be epsilon oxide divided by thickness of oxide.

So, I am ignoring the area part of it. The regular parallel plate capacitor epsilon A by d, A is the area divided by the distance between the plates. We will use capacitance per unit area. This will be having units of farad per centimetre square. So, capacitance you know, and you apply a certain voltage. You know how much charge is going to be there. And if you apply a certain amount of charge on the positive plate, the opposite charge has to be uncovered in the semiconductor.

The holes have to be driven away. And you should have a depletion charge there. So, this is basically the capacitor action leads to what is known as depletion charge. So, this kind of a biasing mode is called as depletion mode. If you take a P-type semiconductor and let us say apply a positive charge it is called as a depletion mode. You are depleting the substrate. You could have another scenario wherein you apply V_A less than 0.

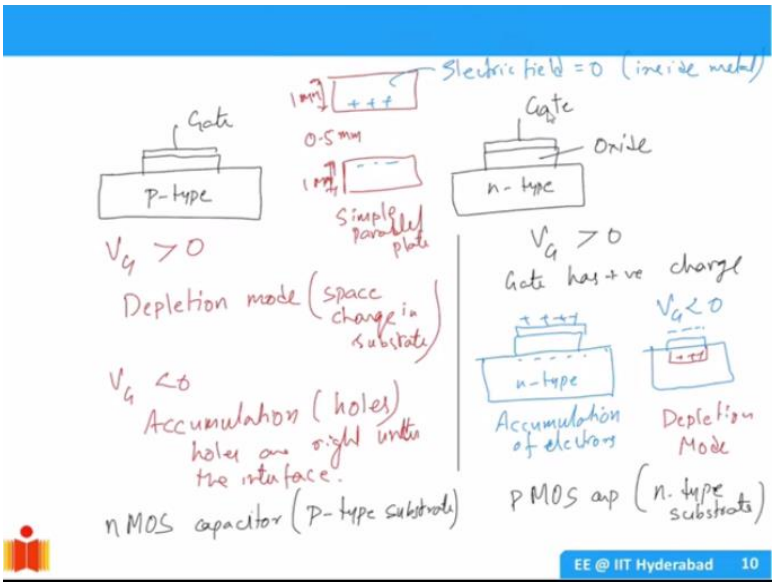
When you apply V_A less than 0, what happens? Well, you have the same substrate. And then there is an oxide. And then on top of it there is a metal. But now, you are adding negative charge on the top. So, that will cause the holes to come closer to the interface. So, if you add a negative charge, what should happen in the substrate? There should be a positive charge. This is known as accumulation. This sort of a regime is known as accumulation mode.

Remember, whenever we say accumulation, we are talking about majority carriers. They are free charges. These are free carriers or majority carriers. So, physically, where will they be? They will be just under the interface whereas depletion charge is space charge, or you know I mean if you want to call it, it is because of dopant ionization. Dopant or you know I will call it charge or ionized dopants.

So, there is a key difference between that the distribution of the charge in the semiconductor. It is not the same. It is not as simple as a parallel plate capacitor. So, we were talking about the depletion and accumulation mode.

And we said that if you have a negative voltage applied on the gate. So, by the way, the metal is called as a gate. And if you apply a negative voltage on the gate, it will create accumulation of carriers in the substrate. This accumulation or depletion is dependent on the type of the substrate you know.

(Refer Slide Time: 08:30)



So far what we have looked at was if you consider a P type substrate and then I will have a oxide and then I will have a metal. So, this I will call as a gate. So, essentially the gate voltage is controlling the type of carriers. That is why we call it a gate. So, now if you have this substrate, you could also have an alternative structure wherein you start with an n-type substrate and then apply. You know there is a oxide. This is oxide.

And then there is a metal on top which I will call as a gate again. So, let us change our notation a little bit. Now, what we have seen is if let us call this as gate voltage V_G. If you apply gate voltage which is positive greater than 0, then if you have a P-type substrate you are going to drive holes away. And then you get to depletion regime depletion mode wherein you have space charge in the substrate.

This is distributed over a certain distance. We are depleting the semiconductor P-type semiconductor. And so, there will be a uniform doping. Let us assume. Then there you will have a charge profile which is distributed in the P-type semiconductor. And if you apply V_G less than 0, you have accumulation of the majority carriers which are in this case holes. And these are located right under the interface.

So, what I was trying to get it is let us say if you have a metal a simple parallel plate capacitor. Let us say you have a parallel plate capacitor consisting of a metal of some millimetres another metal. This is simply the thickness of the metal. Let us say this is 1 millimetre. And this is another 1 millimetre. You have the separation. Let us say it is again you know 0.5 millimetres. Just for explanation.

So, now if I apply a voltage to this, this is a simple parallel plate capacitor. So, where if you apply a voltage, where will the charge be? The charge let us say if you have positive charge here, there should be a negative charge. But where will that physically? Where will the charge be physically? It will be at the edge of the metal because we know from basic electrostatics that there cannot be any charge in the, there cannot be any electric field in the metal.

Electric field is 0, electric field equal to 0 inside the metal, outside non-zero. So, at the interface there has to be a charge which is going to be a plus q. So, this is at the edge. Similarly, in the other plate, there will be negative charge but that is right at the surface not inside the metal itself. What happens in a you know P type you know this sort of a if you have a semiconductor which is P type?

When you deplete it, the negative charge is not really at the surface. But it is distributed within the P-type semiconductor. And if you have accumulation, it is right at the interface, we will draw some space charge diagrams and this will become clearer. But I think this is not very difficult to imagine. So, you have this for a P-type semiconductor. And when you have this sort of a configuration, we will call it as a nMOS capacitor.

It will become clear why we call it. So, if you say an NMOS capacitor, we are talking about a P-type substrate. If I have an n type substrate, what happens? When my gate voltage V_G is greater than 0, what happens in a n-type substrate? Well, gate voltage is greater than 0. So, I am going to have positive charge on the gate. Gate has positive charge.

So, the substrate should have negative charge. Where will the negative charge come from? Well, there are lots of free electrons. n-type semiconductor has lots of electrons. So, you will end up getting negative charge at the surface. If I have this sort of a structure, this is your n

type. And then there is a oxide. And there is a positive charge on this side. So, when you apply a positive charge now, this has become accumulation of electrons.

This is called accumulation mode. Whenever you accumulate majority carriers, you know whether when you have a extra maturity carriers it is called as accumulation. And if you apply V_G less than 0, what happens? When V_G is less than 0, then the gate has a negative charge and that will repel the electrons away from the interface. And it is you have depletion.

But essentially what you have is. So, there is negative charge on the top gate. And then on the semiconductor side, we have space charge which is distributed slight distance away from the interface. So, now, we are depleting the semiconductor. Depletion mode, I can call it. So, you have 2 types of modes. One is accumulation mode; one is depletion mode. It depends on you know if you have a n-type substrate.

We call this as a PMOS capacitor. PMOS cap and NMOS cap. And the behaviour is exactly opposite. For a NMOS cap, if you apply a positive voltage, you get depletion. If you apply negative voltage, you get accumulation of holes. And if you have a PMOS cap, if you apply a negative voltage, then you have depletion.

If you apply a positive voltage, you get accumulation. So, this is the simple picture of what is happening. Now, we would like to understand a little bit more depth. We will want to talk about band diagrams. I will do that in the next video, thank you.