Introduction to Semiconductor Devices

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Lecture - 6.4
An Ideal MOS Capacitor

Hello everyone. Welcome back to Introduction to Semiconductor Devices. In the course, so far, we have studied the operation of p-n junctions. We also looked at p-i-n junction and then Schottky junction. So, today, we will expand our horizon a little bit. We will talk about a device which is known as MOS capacitor.

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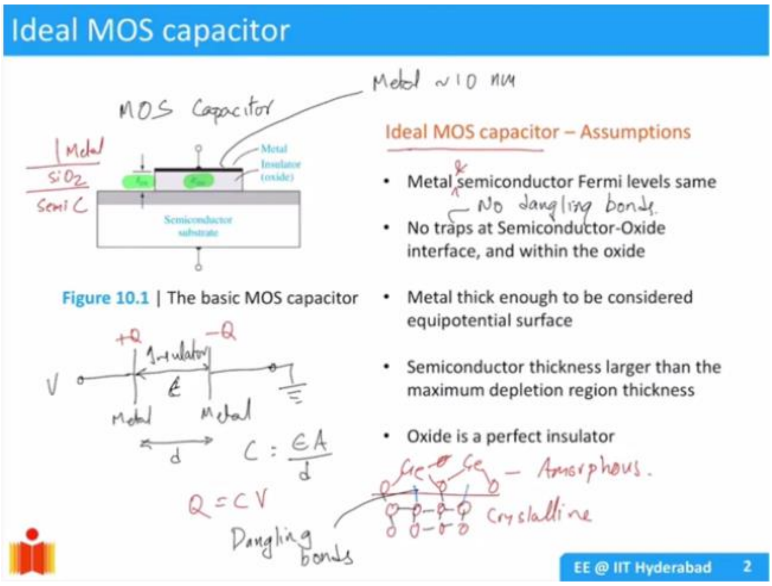

Ideal MOS capacitor

Figure 10.1 | The basic MOS capacitor

Ideal MOS capacitor – Assumptions

- Metal & semiconductor Fermi levels same
- No traps at Semiconductor-Oxide interface, and within the oxide
- Metal thick enough to be considered equipotential surface
- Semiconductor thickness larger than the maximum depletion region thickness
- Oxide is a perfect insulator

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A MOS capacitor is the heart of a modern MOSFET. So, it is still a 2 terminal device. The actual MOSFET will be 4 terminal. We will talk about it after we finish with the MOS capacitor. But this 2 terminal device which we known as which is called as a MOS capacitor gives you the necessary tools to understand the operation of a MOSFET while being simple enough. So, what is a MOS capacitor?

A MOS capacitor is simply a structure consisting of 3 parts. So far, we have looked at only p and n or metal and semiconductor. But, now, we are introducing one more element in between which is an insulator. So, a MOS capacitor consists of a semiconductor. It could be a substrate of wafer. On that you have a thin layer of oxide which is an insulator and then a metal on the top. So, that is why the name MOS capacitor.

MOS, just a moment, MOS stands for metal oxide semiconductor. And it behaves like a capacitor. That is why it is a cap. So, you are all familiar with the regular capacitors. So, you have a 2 terminal device. Let us say I have you know 2 metals that let us say metal and metal. 2 metal plates separated by an insulator. This is an insulator whose dielectric constant could be some epsilon.

And we apply a voltage to this. Now, this is let us say you apply a voltage you know let us say this is grounded. And then you apply a voltage on that. So, we say that this device has a capacitance which is simply going to be epsilon A by d. d is the distance let us say. This distance let us say is d. Then we will say that this capacitor has a capacitance of epsilon A by d. But, what does it do?

It is simply a device which will you know let us say if you apply a positive charge q plus q at a certain voltage let us say we are adding a charge q here, then immediately there will be a minus q charge on the other side. Such, basically, the capacitance is relation between q and V. You apply a certain voltage. The device has a certain amount of capacitance.

So, that extent of charge will be on the plate, plus q on one side, minus q on the other side. This is a simple capacitor that we have studied before. So, now, a MOS capacitor is also similar, but it is one of the plates of a capacitor is a semiconductor instead of a metal. So, you have this top plate which is a metal. This is metal. And then you have a separator you know insulator. This is SiO_2, silicon dioxide right now. We will change it later.

It can be any insulator actually. And then the second terminal or second plate is a semiconductor. So, this is a MOS capacitor. That is why the name. So, in this, one of the crucial parameters is the thickness of the oxide, t_{ox}, we call it thickness of the oxide. And the permittivity oxide, we call it as epsilon oxide. And this is essentially the heart. And to understand this, we will start with several simplifying assumptions.

So, we will call, we will refer to a capacitor which satisfies these assumptions as an ideal MOS capacitor. Of course, you know no real device is going to be ideal. But, for now, to gain the basic understanding, the assumptions that an ideal MOS capacitor has to satisfy are that the metal and semiconductor I should have put here metal and semiconductor Fermi levels are the same. That means let us say we have some doping.

Substrate can be a n-type or a P-type substrate. Let us say it has some doping. The metal also has the same Fermi level. There is no difference in the Fermi levels. Right now, we will make that assumption. This is at the equilibrium with no applied voltage. But if you apply voltage of course the Fermi levels are going to shift. We have seen multiple times. It is not a very severe assumption. I mean we can relax it quite easily.

We will see that in the next week. And then there are no traps in the semiconductor oxide interface or within the oxide. This is a very crucial assumption. It turns out that historically one of the first transistors or semiconductors to be used was germanium. And then when they tried to grow an oxide on germanium, the interface was not very good. By which we mean let us say you have germanium.

Let us say if you take, you will have the germanium lattice, crystalline lattice of germanium which is a perfect crystal. That is all. And then you try to grow germanium oxide on top of it. So, this is going to be germanium. Let us say oxygen and so on. There will be some germaniums which are germanium oxygen. This is an amorphous material. And when you have this interface between crystalline and amorphous, there will be some bonds of germanium.

For example, here, let us say this bond is not paired with any germanium or oxygen. It is left dangling. Or this also could be a bond you know which is not satisfied. Basically, we expect that all silicon atoms are connected. They have this covalence series or silicon or germanium similar. They have they are connected to the neighbouring atoms. But now, it turns out that if you form this interface between a crystalline and an amorphous material, there are some atoms of germanium which are not connected to any atom of oxygen or germanium.

So, these we call it as dangling bonds just to indicate that they are not connected to any atom. So, these are they behave like a trap. And then they actually deteriorate the electrical properties of the device. So, it turned out that even though germanium was actually the one of the first semiconductors to be investigated. The interface between germanium and germanium oxide was not very good whereas the interface between silicon and silicon atom was extremely good.

I mean it has a very low defect density. We will talk about that later. So, we will assume for a moment that ideal MOS capacitor has no traps. So, no dangling bonds. So, these are basically means no dangling bonds which is reasonable for silicon, silicon dioxide. The number of dangling bonds is quite small. And we will study what happens if they are there later on. And also in the interface, there is no charge or no trap basically.

So, it is very common to have some traps within the bulk of the oxide. Now, what do I mean by a trap? It could be simply that you know a bond is not satisfied and then there is a positively charged atom there. And then some negative charge can come and occupy it. Or sometimes you know a positive you know charge could be trapped somewhere it cannot move because of the way the crystal is forming.

So, these are called as you know charge traps. And they actually deteriorate the performance a lot. So, for now, we are assuming that there are no such traps. It is a perfect oxide which is a good assumption to make. And then the metal is thick enough to be considered as an equipotential surface. This is important because I mean when we take the regular you know macroscopic devices, metals are quite thick. We do not have to worry.

But remember, in semiconductor technologies, we are always making the devices smaller and smaller and smaller. When we make them smaller, let us say if I make this, metal 10 nanometres, I made it like this. Do you think that it will behave like a pure metal? Well, of course, no because metal will have something called a surface scattering. The electrons which are flowing in the metal there are no more free electrons.

But, they are scattering with the surface. And then the resistivity increases. Because of this, there is some voltage drops. As the, you know if you apply a piece of volt, you know we calculate the resistivity of metal as you keep decreasing the thickness. At some point when it becomes very thin, the resistivity increases. And there is a voltage drop across the metal. And that can lead to lot of problems.

So, for now, we are assuming that you know metal is thick enough to be considered as an equipotential surface. That means if I apply if I on this metal let us say if I apply at this point some voltage, I am going to have the same voltage at this point. There is no difference between the voltages across. There is no voltage drop across the metal surface. And essentially, it means that the, I mean there is nothing like a skin depth and things like that for a metal.

It is thick enough. So, you do not have to worry. I mean it is much bigger than that. That is what we mean is much bigger than skin depth. Anyway, and the other assumption is that semiconductor thickness is much larger than the maximum depletion region. We will look at this. And generally, this is a very valid assumption. We do not you know this is not very difficult assumption to satisfy.

Because we are dealing with semiconductor wafers which are about 500 microns thick in the past. Right now, they are about 750 microns thick. That means still you know, 750 micron should be three fourth millimetre, three fourth of a millimetre. So, they are quite thick right now. So, we do not have to worry about that. And oxide is a perfect insulator. Well, that is again, we already talked about it.

So, it is said that you know the magic of silicon technology is actually the magic of the interface between silicon and silicon dioxide.

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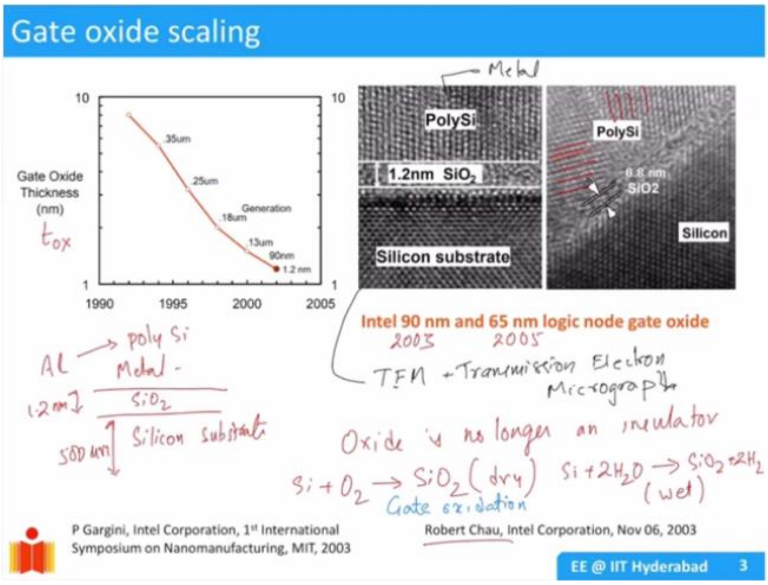

Gate oxide scaling

Intel 90 nm and 65 nm logic node gate oxide
2003 2005

TEM → Transmission Electron Micrograph

Al → poly Si
Metal -
1.2nm SiO_2
500 um Silicon substrate

Oxide is no longer an insulator

$Si + O_2 \rightarrow SiO_2$ (dry) $Si + 2H_2O \rightarrow SiO_2 + 2H_2$ (wet)
Gate oxidation

P Gargini, Intel Corporation, 1st International Symposium on Nanomanufacturing, MIT, 2003

Robert Chau, Intel Corporation, Nov 06, 2003

So, silicon dioxide and silicon interface was so great that electronic device operation has been possible. And one of the big trends in semiconductors has been what is known as gate oxide scaling. Why do I want to talk about that? Well, what happened was, you know we mentioned we introduced this gate oxide. And if you look at the gate oxide thickness in let us say early 1990s, it was you know 8-9 nanometres, 10 nanometres or so.

It is quite high. So, it was a good insulator. And it was a perfect it was a good oxide. But because we wanted to make the transistors work faster and faster, one of the requirements was that the gate oxide has to become thin. You have to make it thinner and thinner. So, in a way, we are scaling, when we are multiplying the gate oxide by a certain number and then we are making it smaller and smaller and smaller.

So, this is what happened in the semiconductor industry over the last you know 30 years. Essentially, we start with you know some thickness of oxide. And then as you come down the thickness was smaller. This is called 350 nanometre technology, 250 nanometre, 180 nanometre. And by the time, we reach 2005 or so, we were at a point you know actually 2003 I would say we were at a point where the thickness of silicon dioxide was 1.2 nanometres.

Just imagine 1.2 nanometres is essentially maybe 5 to 6 atomic layers thick, just 5 to 6 atomic layers. It is not microns. Now, we mentioned that the thickness of a human hair is a few microns, micron or so. 1,000 times smaller than that is 1 nanometre. And effectively, the capacitor we are building is actually with just 1.2 nanometres of silicon dioxide. If I do not know, what else you know? This is magical.

That the fact that, it actually worked is magical. But anyway, so, this is just an image. You know this is what we called as scaling. We will discuss scaling later on when I discuss MOSFETs, we will discuss in greater depth. What is scaling? And, how it improves the performance? Or, how it improves the speed of the MOSFET? We will discuss it later. But, for now, I just wanted to introduce you know in the context of the MOS capacitor.

How does this physically look like? The images you are seeing on the right side you know this is what is called as a TEM image. This is called as TEM image TEM micrograph we call it, Transmission Electron Micrograph. So, essentially what this is showing you is we take a thin slice of the vertical cross section of a MOS capacitor and then shoot electrons at it. And most of the electrons will pass through.

But wherever you have an atom, they do not pass through. So, with this technique, you can actually see the way atoms are arranged in a lattice. And that is what you are seeing here. You see here. This is a silicon substrate on the bottom. And you can see this order you know I will zoom it in a little bit. So, you see these atoms which are arranged. These are the bonds which are forming and atoms are arranged.

You are actually able to see these atoms. The atomic bond length will be like you know 3 to 4 angstroms. And we are able to see that. This is really you know magical. You know at least I get fascinated. You know I it is unbelievable that we can do this. And you see this perfect lattice of silicon. On top of it, you see this. This is the oxide which is an amorphous material. So, you do not see that orientation.

You do not see this perfect lattice arrangement of silicon. You see some random you know silicon and oxygen atoms. And the thickness is just 1.2 nanometres. You might wonder you know how did we take this image? And if you want to take this image there is an equipment called TEM which, is you know few tens of maybe up to 10 million dollars or so. It is a very expensive equipment.

With that you can take this image. And then, so, you have the silicon substrate and 1.2 nanometre oxide. And top of it, in this case, you know what is shown is basically instead of a metal, we are using polysilicon you know. So, in the origin in the back in 19 you know 70s and 80s, we were using aluminium as a metal. So, basically, what is our MOS capacitor consisting of consists of? So, you have in the metal which is some thickness.

Metal in this and then silicon dioxide and then bottom was silicon substrate. So, this would be something like 500 microns thick, half a millimetre thick whereas this is just you know in the initial days in the early 90s it was 10 nanometres or 8 nanometres. But by the time we came to 2003, it was already 1.2 nanometres. And this was aluminium in the beginning in the 80s. But there were certain reasons why you know we shifted from aluminium to what is known as polysilicon.

So, the idea was that if you take polysilicon, we mentioned polysilicon in the first week of the course. You know it is not a perfect lattice or perfect long range order of silicon. I mean you have a perfect crystal silicon, there is long range order. You travel you know 1 millimetre across the sample. You still have the same orientation. It does not change. But polycrystalline is that you have orientation some lattice structure in the domains.

But then if you go long distances, the domains are randomly arranged. That is called as polycrystalline. It has multiple crystals. So, you have this polycrystalline silicon. And then if you dope it highly, it behaves like a metal. It is not a true metal. It is a quasi-metal I would say. But it work like a metal. And there was a reason why semiconductor industry chose polysilicon.

So, physically the MOS capacitor is consisting of this sort of a structure. And you see this. You know this t_{ox} reduce. This is t_{ox}. t_{ox} was scaling from 10 nanometres to 1.2 nanometres. And it turned out that you know this was in 2003 I would say 90 nanometre technology. By the time 2005 came, there was something called known as 65 nanometre technology where the thickness of silicon became 0.8 nanometres.

These are the images taken from a presentation by Robert Chau. He was a one of the Intel fellows. I mean Intel fellow is one of the topmost technological positions in Intel. And then he gave a presentation in 2003. I picked it up from there. You could search on the internet. And you will find it. And the picture on the left was taken from another presentation by one Gargini. He was also an Intel fellow. So, you could look at that.

So, essentially it is another direction. You have this lattice of crystalline lattice. And there is this point, 1.8 nanometre thick silicon dioxide and then polysilicon. And you see here. You see the orientation. I mean see this here. Silicon atoms are arranged in these lines. Here the silicon atoms are in this direction. You have different domains of silicon. That is what we mean by polycrystalline silicon.

So, when the transistors became such small sizes or you know when the MOS capacitors became the thickness of the oxide became very small there were problems. There were a lot of problems as such. One of the biggest problem was oxide is now no longer an insulator. When is it an insulator? You know it has this band gap. But the problem is very thin. So, electrons used to tunnelling above the oxide.

You know we talked about barriers and a potential barrier. And across the potential barrier, the electrons can tunnel and give rise to current. So, if you have a capacitor and you have a leaky oxide. Oxide became leaky I would say, if the oxide is leaking then the transistor action will not work. The MOS capacitor will not work perfectly. This was one of the great challenges of the time. And this was solved again by Intel in 2007.

And just when I was about to finish my master's you know best that Intel announced that there is this High-K metal gate. And we will talk about that later in the week. So, right now, so, this is how actual a MOS capacitor looks like. And how did we achieve this silicon dioxide? No silicon, I told you that you know you have this silicon dioxide. We take and mix it with carbon. And then you can form silicon.

And then you purify it you know by using a very elaborate series of steps. And you get this wafer which are perfectly pure silicon crystals. So, they have about 9 impurities what we mentioned. So, now, how do we form silicon dioxide? Well, it turns out that there are 2 processes to form silicon dioxide. One of them is called as dry oxidation wherein I simply mix silicon and oxygen in a dry oxygen. And then I form silicon dioxide.

And this is called as dry oxidation. So, basically you pass gas of oxygen and on a wafer of silicon, heat it up and then you form silicon dioxide. There is also another process which is called as wet oxidation. Wherein, I use water vapour H_2O, if I pass, then I get SiO_2 plus $2H_2$, I think. So, basically instead of passing oxygen vapour, you pass water vapour. And this is called as wet oxidation.

If you are to study the VLSI technology, they will tell you that this is the process gate oxidation is done by dry oxidation process. So, if you just pass dry oxygen just oxygen no water vapour, then you will get very high-quality oxide whereas if you do wet oxidation, you get low quality oxide. But you can get a very thick oxide. Dry oxidation is a very slow process. So, you cannot make a very thick oxide.

But you know in gate, we just want 1 nanometre oxide. So, dry oxidation is a perfect process for that. And using dry oxidation, we make this oxide on silicon wafer. And then you deposit metal on top of it. That is how you make a MOS capacitor. So, this was a brief overview of the structure of MOS capacitor. And in the subsequent videos, we will talk about the electrical properties.

You know how to understand the electrical properties? And so, we will meet you in the next lecture, thank you.