Introduction to Semiconductor Devices
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Lecture – 5.6
Non-Idealities in PN Junction Diode

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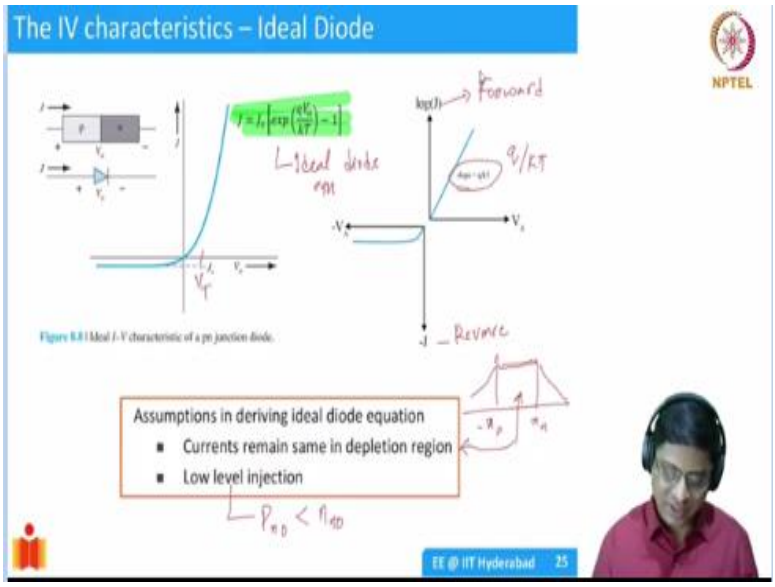

Welcome back. The last topic, I want to cover in PN junctions is the differences between an ideal diode and a non-ideal diode. So far, what we are seeing is what we refer to as an ideal diode and the expression that we have derived is current density,

$$J = J_s[\exp\left(\frac{qV_a}{kT}\right) - 1]$$

This is actually called as ideal diode equation.

Well, you know because, it is an idea that because we have made some assumptions and those assumptions are that, when we are calculating the currents, we had the depletion region. So, we had this $-x_p$ and x_n. We looked at the depletion currents here and here. But we said that there is no change in the depletion region currents.

But well, you are introducing holes and electrons, excess holes and electrons across the depletion region, so there is going to be some recombination happening. And there is also going to some generation happening because it is completely depleted of carriers. So, there are some generation recombinations that can happen in the depletion region, which we have ignored. And today, we will see the effect of that.

And also, we assume that we have low level injection, by which we mean, let us say you are injecting number of holes into N type semiconductor, we said that the injected excess carriers are still going to be less than the majority carriers or n_{n_0} . n_{n_0} means electrons in the N type semiconductor at equilibrium. So, it is still going to be less.

But if you try to inject more holes, then we are going to have a region where you know, even the majority carrier concentration is going to be perturbed and then your current characteristics will be slightly different. So, we made these assumptions and we derived this and you must be familiar already with this sort of a diode like action. You know, it is kind of linear in the small voltages. In a finite range, it is going to be linear and there is this threshold voltage that we can define V_T .

So, to understand the non-idealities, we will try to plot it in a slightly different form. So, I will plot it in such a way that, in the forward bias, I am plotting log of current ($\log(J)$)versus applied voltage. In the reverse bias, I am just plotting the linear current versus linear voltage. It is just a mixed graph. That is why the small break in axis. So, if you take a logarithmic J or take the logarithm of current, what you will get?

You essentially will see that the slope is going to be $\frac{q}{kT}$. So, you are going to get a straight line if it is an ideal diode. And we will quickly show that this is never going to happen. So, one of the first non-idealities that I would like to discuss is what is known as a junction breakdown.

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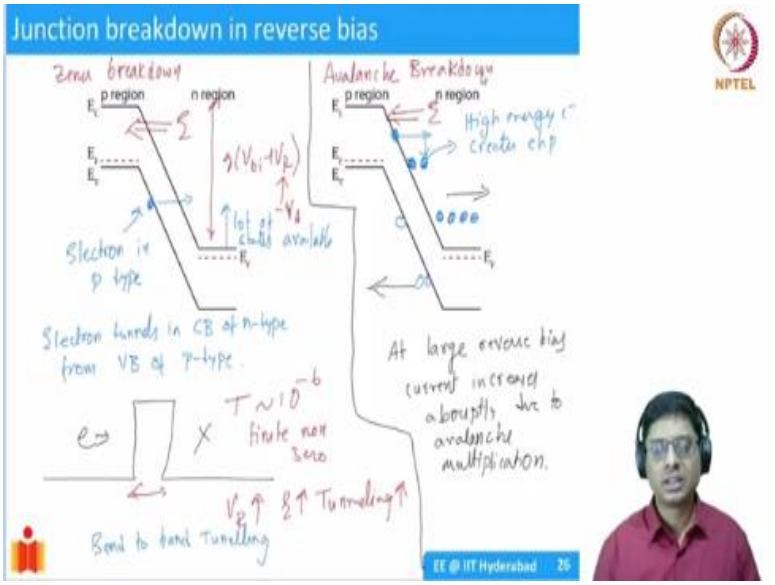

So, we are applying the reverse bias voltage into the PN junction. And we are assuming that this current is going to be constant like this. And we never specified how long it is going to remain constant. But it turns out that after a point, the diode breakdown is a sudden increase in the current. This particular phenomenon is called as junction breakdown. So, you cannot simply keep extending the depletion region as much as you want.

At some point, it is going to breakdown and what is that point you will see. So, to understand the junction breakdown, we have 2 processes that are important. The first process is what we known as the Zener breakdown. And the second one is called us avalanche breakdown. So, what happens is Zener process? Let us say if you increase your depletion width or you apply more and more reverse bias voltage, your banks are going to become steep because you are going to have larger and larger electric field.

So, there is more charge uncovered. So, larger peak electric field, so more band bending, so bands will bend. And this is a schematic illustration of how the bands could bend. Basically, you have a large barrier which was $q(V_{bi} + V_R)$. And assuming that V_R is basically $-V_A$ and V_A is negative so V_R going to be positive; the total is going to be positive.

So, it is going to have a large barrier. Now, what happens if you have such a large barrier? It turns out that you have at position; for example, here if you look, you have a large concert, you can have basically the valence band is full of electrons. So, electrons are all bonded to the lattice. If an electron is absent, then we call that as a hole, but in principle, you have lots of

electrons and the electric field is directed in the negative x axis. This is the direction of electric field.

So, in principle, your electron can actually go from the valence band into the conduction band of N type. So, this is basically electron in P type semiconductor. And here, you see, we are studied as you go deeper, lot of states available. It is an empty; you have a lot of states in the conduction band available. So, what is going to happen is your electron is going to go into the conduction band of the N type.

So, this process basically is called as tunnelling. So, electron tunnels into CB of N type semiconductor from valence band of P type. Remember, we mentioned tunnelling in the first couple of lectures in passing, actually. So, what is the tunnelling? This is an energy barrier, as you increase the voltage, the energy barrier becomes narrower and narrower that is all.

But, you still have a barrier. So, essentially, if you have an energy barrier like this and you have an electron incident on it, what happens? We said that in classical mechanics, they should not be any probability of finding electron here. But quantum mechanically, there is a certain finite tunnelling probability, it could be 10^{-6}, something that 10^{-4}, whatever, there is going to be some finite nonzero.

What happens if you have the probability? Well, if you have 100 electrons, one of them is going to come and valence band is full of electrons. We have 10^{22} that is the number of lattice atoms and each of them has 4 electrons. So, they can tunnel into the other side. So, there can be a lot of current that can flow. And this depends on the barrier width.

If your electric field is increased or rather applied voltage is increased, as V_R increases, electric field increases because the gradient is stronger and because of that tunnelling increases. So, this current is called as Zener breakdown current. We call it also band to band tunnelling; it is just a fancy name of saying. Essentially saying that from valence band of P type to conduction band of N type that is a band to band tunnelling. So, this is Zener breakdown.

We also have another type of breakdown, which we call as avalanche breakdown. We have already seen that. Here, there is an electric field. This is the strong electric field here. And

whenever you have an electric field, the carrier requires a lot of energy as it travels; we have seen the kinetic energy of the carrier. So, if you let us say take an electron, let us say from here, it is going to travel and it is goes deeper, it has a kinetic energy.

And with that kinetic energy, it can knock off an electron from the lattice. So, what it can do is, it can take for example, an electron it can knock off from the lattice and create a hole in the valence band and create an electron in the conduction band. And then there is also the original electron. So, basically, high energy electron creates electron hole pairs, 1 electron as it requires kinetic energy to create 1 electron hole pair. It depends on the amount of energetic it requires.

And then these 2 electrons will travel again in the band, the conduction band, they are free to move and as they acquire kinetic energy, they create more holes and then you end up getting more electrons. So, this process basically 1 electron will create 2 electrons; 2 electrons will create 4 electrons and 4 will create 8 electrons and so on; it just multiplies. It depends on how many carriers, how many electrons it is creating multiplication factor, we call it. For each electron, how many new electrons are being created?

Of course, they are going to be holes also created and holds effectively will go in this direction. Electrons will go in this direction and keep getting multiplied as it travels across the crystal. So, if you have a large reverse bias, current increases abruptly due to avalanche multiplication by which means that essentially each electron is going to create more electrons and so on. That is why we call it avalanche.

So, this is called as avalanche breakdown. These are the 2 main junction breakdowns that we see in the PN junctions. And how does it reflect in that IV curve?

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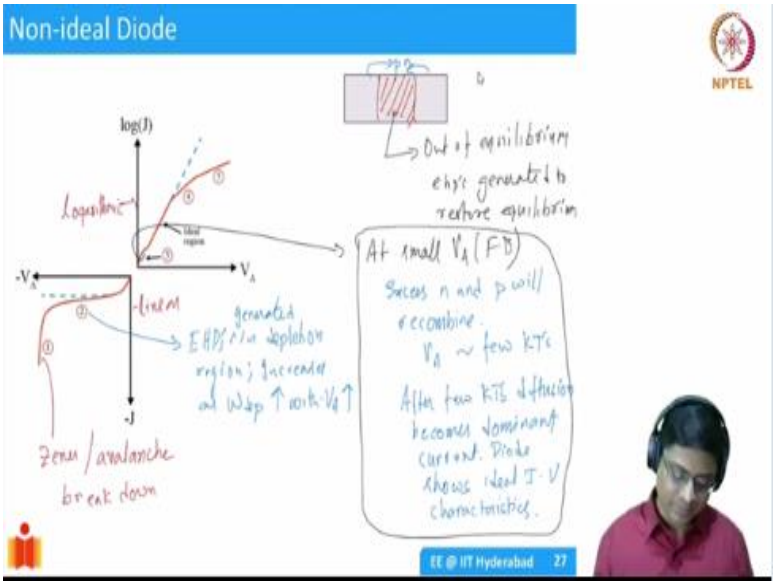

Well, we saw the initial ideal IV which was in the blue. Now, I made a dashed curve here. If you have junction breakdown, we see that in the reverse bias after some point, it simply increases. This is basically called as breakdown. It could be either Zener or avalanche breakdown, what exactly depends on the voltage in the sense one which is not important for us. The second type of non-linearity that I would like to discuss is basically the electron hole pair generation in the depletion region.

So, what happens? Let us say you have a PN junction. Let us say, I have a PN junction this way and I have a depletion region in between. I apply reverse bias and then the depletion width increases but, this is essentially out of equilibrium. Whenever semiconductor goes out of equilibrium, it tries to come back to equilibrium. When you have excess minority carriers, they will recombine.

When you have less carriers, it will generate. So, EHPs generated to restore equilibrium. So, if you have electron hole pairs getting generated, you know we said the reverse saturation current. This was due to the availability of minority carriers. On the Quasi neutral regions, you will sweep away whatever carriers are available into the other side that is how reverse saturation current was coming.

But in addition to that now, we have electron hole pairs which are getting generated in the depletion region itself and as the depletion region width increases, more and more carriers are going to get generated. So, this leads to one form of non-ideality which we call as EHPs

generated in depletion region, which we identified section-2, basically, this increases as W_{dep} increases with V_A increase in the negative direction.

As you go to more and more negative voltages, the depletion width increases. So, more and more electron hole pairs are getting generated and that is why there is this gradual change in the curve. So, this section we call it as electron hole pair generation in the depletion region. And the opposite phenomena happen at small gate voltages in the forward bias.

So, you see here, this was at small V_A (forward bias), not reverse. What happens there? They are essentially injecting minority carriers. So, you are bringing in holes here and you are bringing in electrons from this side. So, they are going to recombine. So, excess N and P will recombine. But this effect is not very significant. It occurs at very, very small applied voltages of the order of you know few kT's. If you go to 100 millivolts or something, this is going to vanish.

The reason is the diffusion current goes exponentially. So, once the diffusion current takes over, you know after few kT's moments, 1 kT is basically 25 milli electron volts, few kT's let us say, 100 milli electron volts; after 100 milli electron volts or in a 0.1 volts, diffusion is going to take over; diffusion becomes dominant current and hence, diode shows ideal IV or JV characteristics.

So, this is basically the region 3. So, as this is a third non-ideality that you will see, but, I would say that this is not very significant effect because there is a lot of forward bias current; diffusion is very strong, we saw that it can be few amps per centimetre square.

It was significant in the reverse bias because the current was Pico amps per centimetre square and then any small addition is going to show up and remember this is actually linear, left side graph linear and left side graph is logarithmic. So, you will not see much of change. It is only a small tiny blip in the small gate voltages and then you have the ideal current voltage relationship.

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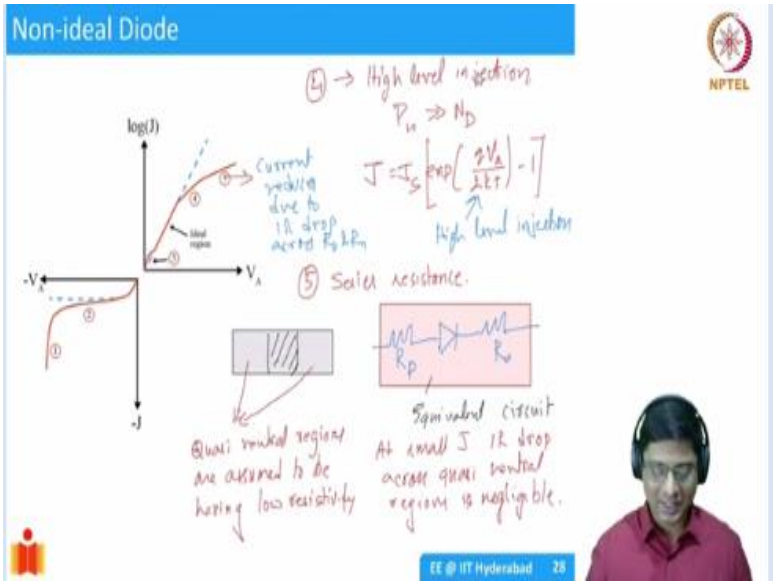

Well, as you keep increasing, you get into another type of non-ideality; after a certain voltage you get into a certain non-linearity which we call as high level injection. Here, region 4 is what we call a high level injection. So, p_n is hole getting introduced into the N type semiconductor. N_D was a donor density. So, number of electrons in the N type is N_D. So, if p_n is actually greater than N_D, then we get into a region which we call as high level injection. And the analysis becomes slightly more complicated, we will not really get into it, we will simply say that now in high level injection,

$$J = J_s[\exp\left(\frac{qV_a}{2kT}\right) - 1]$$

It is only applicable at very high gate voltages.

In the normal gate, you do not need to worry about it. But at high level high gate voltages, you have to take into account and we are not proving it also. We are not even trying to show you why that is; just say that this is what it is. Otherwise, we will have to go into all sorts of complications.

The last known ideality, we can talk about is what is called as series resistance. Well, we have a PN junction. Let us say, you have a PN junction of this form and you have a depletion region. We always worried about the junction you know, carrier dynamics. We never considered what happens in the Quasi neutral regions. So far, the quasi neutral regions assumed to be having low resistivity. Well, it is okay. It is a reasonable assumption for many cases, but the moment you go to very high currents as you go to high voltages, you are getting into high currents.

When you have high currents, effectively the diode turns out to be, in addition to this simple diode. We have an additional series resistance. So, which is going to be R_P and R_N. So, this is my equivalent circuit of the diode. At low currents(J) at small currents, the IR drop across the Quasi neutral regions is negligible.

But once you go to large voltages, the drop becomes significant and then current starts reduce; here, current reduces due to IR drops; IR drop across R_P and R_N, basically systems of Quasi neutral regions. So, that is why you have the fifth type of non-ideality that you can see. Why are we discussing all this? Well, I mean, I could simply talk about PN junctions and then say that you know, the threshold voltage is you know, whatever log $\left(\frac{N_A N_D}{n_i^2}\right)$ and so on and finish it up.

But then all these small things matter, when we look at what is known as VLSI, very large scale integrated circuits; in that all these non-idealities come into picture and we have to study. So, as part of foundation course, I just wanted to tell you the ideal diode behaviour, which you have done most of the time, but we just took 30 minutes to analyze what happens, what are the different non-idealities that are present.

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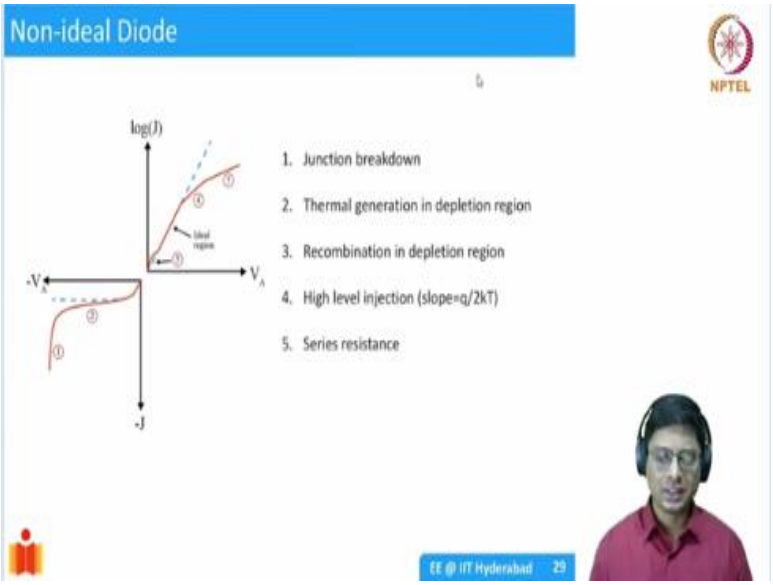

So, to sum up, these are the non-idealities, which I have already written down, we can just go through it one more time.

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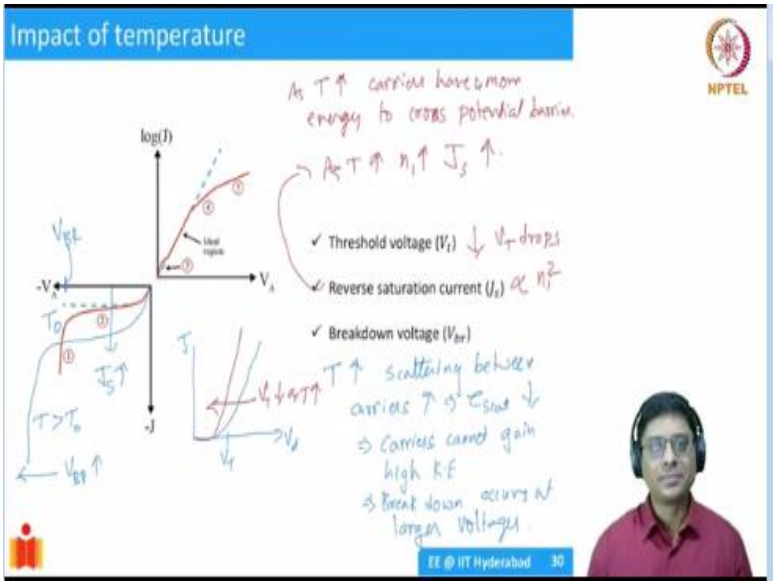

So, before I stop, I just want to mention one more aspect, which is important, which is the impact of temperature. So far, in the PN junction analysis, we have not changed the temperature, but you could change the temperature in a real device. For example, if you are taking a semiconductor chip in a computer, if you run it faster or if you run it, you put a lot of load, you run a lot of computations on it, it is going to heat up.

When it heats up, the junctions parameters are going to change, even the threshold voltage is going to change. So, we need to understand what happens to this parameters with temperature. And we will not really go in any depth; we just briefly tell you that. So, essentially, if you increase temperature, as temperature increases, what happens? Carriers have more energy to cross the potential barrier.

So, the threshold voltage reduces; V_T drops as temperature increases. What happens to reverse saturation current? Well, we showed that reverse saturation current was proportional to n_i^2. And that is going to be significantly dependent on the temperature. So, as you increase temperature, n_i is going to increase dramatically and that is why J_s will increase.

The last thing, we need to analyze this, what happens to the breakdown voltage? Well, I probably did not introduce what is breakdown voltage. The point at which this breakdown is occurring, it is called as V_{br}. So, at that point, the current in the reverse bias has dramatically increased. So, what happens to the breakdown voltage as you increase the temperature? Well, this is a little bit more subtle.

Let us say if you have impacted if you have avalanche process, avalanche multiplication happening. So, essentially a carrier is gaining kinetic energy and then transferring it to the lattice and creating electron hole pairs. But if you increase temperature, the carriers are going to scatter much more the scattering time reduces, because of which the efficiency of the multiplication process, avalanche multiplication process is reduced.

So, that is why as T increases, scattering between carriers increases that implies tau, which is basically the time between scattering events. τ_{scat} basically, time between scattering events reduces that means there is more efficient scattering and that is why this implies carriers cannot gain high kinetic energy.

Before the gain, they simply collide with some other carrier and lose energy. So, there is no directionality that is built up because of this repeated scattering events. So, this implies breakdown occur at larger voltages. So, of course, if I did not show you the, you know, in this picture, it is difficult for me to show the V_T, but in the reverse bias, if temperature increases, your curve will look something like this.

If this orange curve was T_0 and this is T greater than T 0 so, J s increases, V_{br} increases, V_T reduces. So, if you have drawn in the forward bias, you know if your normal V applied versus J if you draw, this was your forward bias. This was your V_T and as you go to higher temperature, the V_T will become something like this. So, V_T decreases as T increases. So, this is the final thing that I wanted to talk about.

So, with that, I hope that you know, I have covered a wide range of diode related fundamentals. So, please take your time and then study these things.