

**Introduction to Semiconductor Devices**  
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**Lecture – 5.5**  
**Depletion Capacitance in PN Junction**

This document is intended to accompany the lecture videos of the course “Introduction to Semiconductor Devices” offered by Dr. Naresh Emani on the NPTEL platform. It has been our effort to remove ambiguities and make the document readable. However, there may be some inadvertent errors. The reader is advised to refer to the original lecture video if he/she needs any clarification.

Let us get started. So, in the last lecture, we studied the current flow in a PN junction. So, today, let us start by asking a very simple question: is a PN junction, we also call it a diode, PN junction diode, a linear device or nonlinear device? To understand that we; will have to analyze the current voltage characteristic. For a linear device like a resistor, the voltage is proportional to the current.

What happens in a semiconductor diode PN junction diode? Well, it is nonlinear, because we saw that the current is going to exponentially depend on the voltage. So, it is a nonlinear device. If it is a nonlinear device, can we describe it in the form of resistances and capacitances? Can we model it as a combination of resistances and capacitances? Because if you remember, in the forward bias, you know after the threshold, the current seems to change linearly.

If you go to very large voltage ranges of course, it is going to be an exponential; truly exponential, but then you could approximate it by a fixed resistance. So, current in the vertical axis; voltage in the horizontal axis, you see that above the threshold, it is sort of a straight line; you can try to model it. So, is there any capacitance associated with the diode? That is what we would like to answer. Why are we interested in capacitance?

Well, it turns out that the product of resistance and capacitance is one of the most critical parameters in the operation of electronic circuits. We have already studied. You must have studied in the basic circuit's course; RC represents the delay. So, if the product of R and C is large, the electronics cannot work at a very fast speed.

So, because essentially, when you say when you look at an electronic chip, be it a mobile phone or a computer or laptop, essentially what you have is digital gates, which are working with zeros and ones. And there is a continuous switching between 0 and 1. And we are trying to compute. So, all the numbers are being represented in binary in the form of zeros and ones.

And then you do computations on that and that is why you have a computer. So, the speed with which you can make these calculations is going to determine fundamental on the product of R and C. So, we would like to understand whether the diode has a capacitance associated with it.

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The slide, titled "Capacitance of a PN junction", illustrates the derivation of the junction capacitance. It features several diagrams and equations:

- Top Left:** A schematic of a PN junction with P-type (N<sub>p</sub>) and N-type (N<sub>n</sub>) regions. A voltage V<sub>b</sub> is applied across it. The capacitance is defined as  $C = \frac{dQ}{dV}$ .
- Top Right:** A cross-sectional diagram of the junction under reverse bias. The depletion width is labeled as  $W_{dep}$  with  $V_b$  and  $V_b + dV$  indicated. Charge elements  $+dQ$  and  $-dQ$  are shown on the depletion edges.
- Middle Left:** A boxed equation:  $C = \frac{dQ}{dV} = \frac{\epsilon_s \epsilon_0}{W_{dep}}$ .
- Middle Right:** A boxed equation:  $C_{dep} \propto \frac{1}{\sqrt{V_b + V_b}}$  with units  $F/cm^2$ . A note below it says "Voltage dependent capacitor".
- Bottom Left:** A diagram of a parallel plate capacitor with plates of area A and separation d. The capacitance is given as  $C = \frac{\epsilon A}{d}$  and  $C_{unit area} = \frac{\epsilon}{d}$ .
- Bottom Center:** A boxed equation:  $Q = \frac{1}{2} N_A x_p = \frac{1}{2} N_A \frac{N_n}{N_n + N_A} W$ .
- Bottom Right:** A boxed equation:  $W = \left[ \frac{2 \epsilon_s \epsilon_0 (N_n + N_A)}{N_n N_A} (V_{bi} - V_b) \right]^{1/2}$ .

And it turns out that there is definite capacitance in a diode and at least in one of the forms, it is relatively simple for us to analyze. So, look at. Think about this. So, you have a PN junction with an applied voltage. And for now, we will consider the reverse bias. We will not look into forward bias; only the reverse bias. So, what happens in the reverse bias? What is often a capacitance?

Capacitance is simply  $dQ/dV$ . I take a piece of you know, let us say, a parallel plate capacitor I take, I apply a certain voltage, I make a small change in the voltage, I will see that the amount of charge on the plates is going to change by delta Q. So, the derivative  $dQ/dV$  is essentially your capacitance. So, if you have a parallel plate capacitor, this is linear, so it is  $C = Q/V$ . That is why  $Q=CV$ .

So, that works for a simple parallel plate capacitor. But for a diode, we need to analyze what happens to the charge as you change the voltage. That will give us the capacitance. So, how do

we do that? Let us go back to the basics. And let us look at the space charge diode. What we will do is: we will just say, let us say we will apply a voltage  $V_A$ , we will consider that and then we will change that voltage to  $V_A + \Delta V$ .

What happens to the charge? So, without all this, if we will look at the PN junction, you will have as a function of  $x$ , you have something and then you can plot a row. We have done it multiple times already. So, what will we see in this situation? We will see that there is a space charge in the N type region which is going to be positive. And there is a different width, negative space charge in the P type semiconductor.

And we call this as  $x_n$ . And this is  $-x_p$ . The junction is  $x = 0$ . So, now, what we want to understand is: this is at a certain voltage. So, let us say this is the width, let me put this here, I raise this small thing here. And I will say that this is my width  $W_{depletion}$ , applied voltage  $V_A$ . Now, I changed my voltage, I will make it  $V_A + \Delta V$ .

What would what you expect? Let us say it is increasing. We understand that we are applying the reverse bias. So, we are having a larger reverse bias. We know that the depletion width increases. Why should it increase? Well, essentially, the external terminals are going to draw the carriers out because of which the space charge has to increase. So, what will happen?

Let us say, this will increase to this point. So, this is additional  $\Delta Q$  that is introduced due to  $\Delta V$ . And this is also same. This is going to  $-\Delta Q$  that is introduced. So, what happened? As a result of application of an additional voltage  $dV$ , the depletion region has become wider. So, this is my new width  $W_{depletion}$  with  $V_A + \Delta V$ . So, once I know this, I can compute what happens to the capacitance.

What is the width of a depletion region?

$$W = \frac{2\epsilon_{si}}{q} N_a + \frac{N_d}{N_a N_d} (V_{bi} - V_a)$$

$$W = \frac{2\epsilon_{si}}{q} N_a + \frac{N_d}{N_a N_d} (V_{bi} + V_r); \text{In Reverse Bias}$$

So, as you increase the reverse bias voltage, it will simply increase the depletion width. So, what is this change in charge  $dQ$ ? If we do that, we know the capacitance.

So, to compute that, what we have to do is, remember, what is the charge? And before we do that, please think about why I increased it like this. Why not I keep the width constant in increase my space charge. So, there is a reason why specifically, I am drawing it like this extension, I am extending the depletion region, but not increasing it on the vertical axis. Why is that? Think about it.

I mean, it is very clear, you should be very clear by now that it is uniform doping, so you cannot change the y axis. This is going to be determined by your  $N_d$  and this is going to be determined by  $N_a$ . That is the lattice fixed charge. We can only change the extent to which you remove the electrons or holes. For the x direction, you can change. Let us come back to the charge. What is the charge?

$$Q = qN_a x_p$$

$$Q = \frac{qN_a N_d}{N_a + N_d}$$

You see, now we have managed to bring in the width as voltage dependence.

So, now all I have to do is simply compute capacitance:

$$C = \frac{dQ}{dV}$$

$$C = \frac{\epsilon_{si}}{W_{dep}}$$

The total capacitance of a PN junction is simply the dielectric permittivity divided by the depletion width. It should actually surprise you; I mean it looks very deceptively simple. Remember, if you have a parallel plate capacitor with you know, + Q and - Q, what was the capacitance?

$$C = \frac{\epsilon A}{d}$$

There is no reason for us to expect that, the depletion capacitance should be epsilon divided by the width of the depletion region.

In the parallel plate case, you have 2 unique charge plates, + Q and - Q. But in a PN junction, you have a distributed charge. The charge is not at one location  $x_n$  or  $x_p$ . It is distributed over a region from 0 to  $x_n$  and then from -  $x_p$  to 0.

If you had a parallel plate capacitor, it does not exhibit any voltage dependence. It is simply dependent on the material parameters and the distance between the plates.

Whereas if you have a PN junction capacitance  $C_{depletion}$ :

$$C_{depletion} \propto 1/\sqrt{V_{bi} + V_r}$$

So, this is a voltage dependent capacitance. What are the uses?

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The slide, titled "Capacitance of a PN junction", contains the following content:

- Equation 1:** 
$$C_{dep} = \frac{\epsilon_{si}}{\sqrt{\frac{2\epsilon_{si} N_A + N_D}{q N_A N_D} (V_{bi} - V_A)}} = \frac{\epsilon_{si}}{W}$$
- Equation 2:** 
$$C \propto \frac{1}{\sqrt{V_{bi} + V_r}}$$
- Equation 3:** 
$$\frac{1}{C_{dep}^2} = \frac{W^2}{\epsilon_{si}} = \left( \frac{2}{\epsilon_{si} q N_D} \right) (V_{bi} + V_A)$$
- Diagram:** A diagram of a one-sided junction with a linear depletion region. Handwritten notes include "Assume  $N_A \gg N_D$  one-sided junction" and "Figure 1.11 (b) shows  $V_A$  of a one-sided doped pn junction".
- Logos:** NPTEL logo in the top right and IIT Hyderabad logo in the bottom right.

One of the important points is. So, if I look at capacitance, as I said, just a moment back, it is 1 over root of voltage. If I write  $V_A = -V_r$ . And applying reverse bias that is all I want to explicitly make it clear.

So, then I can compute what is  $\frac{1}{C_{depletion}^2} = \frac{W^2}{\epsilon_{si}} = (2/\epsilon_{si}qN_d)(V_{bi} + V_r)$

The text in **red** above is the slope. The reason, this is useful is: we can measure it experimentally. We can apply a reverse bias voltage and keep measuring capacitance at different points.

We have what is called an LCR meter that is used to measure the capacitance. And so, if you measure that and plot voltage versus  $1/C^2$ , you get a slope. And from the slope, you can find out what is the carrier density in your semiconductor, because doping density is something dictated by you know, the doping process.

It is done by the manufacturer. But you can fabricate a device and actually verify what is the doping concentration? So, this is one of the uses. And of course, if you extrapolate it to the x axis, you get the built-in voltage. So, this is a very powerful technique to actually find out the material, the doping concentration and the built-in potential for a PN junction that is where it is used.

So, let us say you know, why do I want to know this? RC is going to influence. My capacitance now, if you calculate it, it will turn out to be a few picofarads/centimetre square or something like that. And then let us say if I fabricate a device, which is having a diode which is having 5 centimetre square area, a large diode, if I do that, the capacitance is going to be large. And because of it, it is going to be slow.

And this is one of the reasons why semiconductor devices are always you know, over the last 50 years, they have been continuously shrunk in size so, much so that. Today, we have only a few you know the MOSFET, which are 5 nano-meters technology or 7 nano-meter technology. So, they are very, very small devices. The reason for that is once you make it smaller, the capacitance reduces; RC reduces so that circuits are faster. That is one of the primary driving forces. So, let us take you know a few numbers and see what it is.

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**Example problem**

Objective: Calculate the junction capacitance of a pn junction.  
Consider the same pn junction as that of Example 7.3. Again assume that  $V_b = 5\text{ V}$ .

**EXAMPLE 7.5**

$$W = \left[ \frac{2\epsilon_i}{q} \frac{N_A + N_D}{N_A N_D} (V_{bi} - V_a) \right]^{1/2}$$

$$\sim 0.5 \mu\text{m}$$

$$C_{j,p} = \frac{\epsilon_i}{W} = \frac{11.7 \times 8.85 \times 10^{-14} \text{ F/cm}}{0.5 \times 10^{-4} \text{ cm}}$$

$$\sim 100 \times 10^{-10} \text{ F/cm}^2 \sim 1 \text{ pF/cm}^2$$

"Diffusion capacitance" → Forward bias

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Well, this is again a problem from the textbook 7.5. You can go back and verify the solution as well. And you are asked to calculate the junction capacitance for a PN junction assuming, all the parameters are not given, but they are all from another example. So, if you are asked to calculate the junction capacitors, first thing you will do is simply the width of the depletion region:

$$W_{dep} = \sqrt{\frac{2\epsilon_{si}}{q} \frac{N_a N_d}{N_a + N_d} (V_{bi} - V_a)}$$

$$= \sim 0.5 \mu m$$

C depletion:

$$C_{dep} = \frac{\epsilon_{si}}{W} = 11.7 * 8.85 * \frac{10^{-14}}{0.5 * 10^{-4}}$$

$$= \sim 100 * 10^{-10} \frac{F}{cm^2}$$

We only talked about the depletion capacitance. You might ask, what about the forward bias? Is there any capacitance? It turns out that even in the forward bias, there is a capacitance which we call as a diffusion capacitance. This is in the forward bias.

The functional behaviour is different. It is essentially something to do with how much time the minority carriers are going to spend in the semiconductor. So, it is related to the minority carrier recombination time. And it is a little bit involved for us right now. It turns out that you know, the depletion capacitance is much more you know, widely applicable.

There is reason for that. You know, when we come to MOSFET, we will talk about it. So, we will not really be talking about diffusion capacitors in this course, other than to say that it exists. But in a lot of cases, you will have the PN junctions in depletion mode in a MOSFET that is why we focus on that. That is going to be much more significant for us. So, I hope that you know, you understand the importance of capacitances.

And then you are able to compute the capacitances for a simple PN junction. So, when we talk about MOS capacitors, we will really use these capacitances you know, left and right, I mean we cannot describe without that. So, please make sure that you follow it. If not, go back and review this lecture. And I will see you in the next video. Thank you.