**Introduction to Semiconductor Devices**
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**Lecture - 5.1**
**Forward and Reverse Biased PN junctions**



Hello everyone, welcome back to Introduction to Semiconductor Devices. In the last week, we have introduced the basic concepts of PN junctions. We looked at the electrostatics. So, you should be able to now compute. You should be able to define what is the depletion layer and then calculate the electric field in the depletion layer and also the built in potential that you see across a simple PN junction without any applied bias.

So, in this week, we will understand what happens to your PN junction when we apply an external bias.

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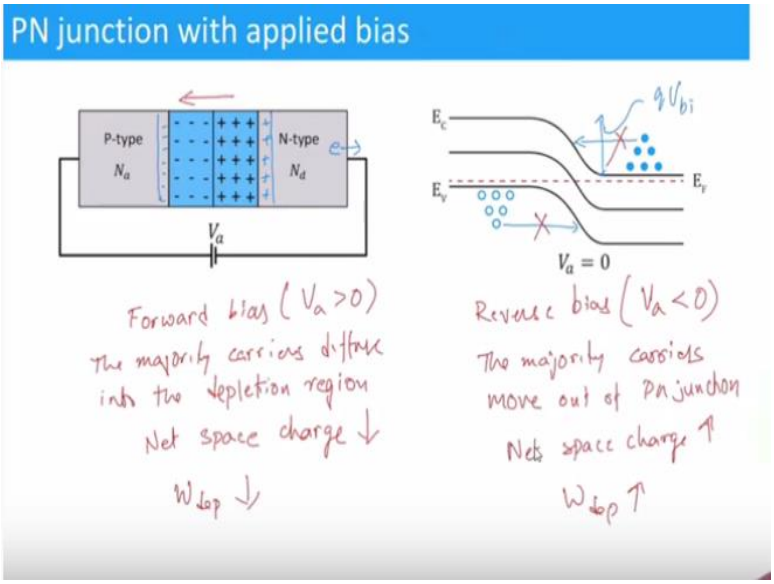


So, you have already seen this. So, you have this P and N regions in contact to form a PN junction. And then there is a depletion region with positive donor charges and then negative accept the charges. Now, if you connect a battery to this PN junction, what would happen? So, this is my external battery, I connect it in such a way that the higher potential is connected to the P type semiconductor.

The lower potential is connected to N type semiconductor. When this applied voltage is 0, then essentially the semiconductor the PN junction is in equilibrium. So, we should see that the Fermi level is uniform all across the PN junction. We have already seen this. And we defined this you know quantity as the built in potential $qV_{bi}$ built in voltage times the charge will give you the electron volts the potential barrier in electron volts.

In addition, newly added symbolic representation of electrons and holes. So, here you see that there are these electrons which are there in the conduction band of the entire semiconductor. And as you go away from $E_C$, you see that there are fewer number of electrons just to symbolically capture the idea that there are lesser number of electrons deeper in the conduction band. Similarly, we are showing holes in the valence band.

You will see that the number of holes reduces as you go deeper into the valence band. And now, if there is no external voltage, would there be any current in the circuit or in the junction? Well, no, the reason is this electron cannot go I mean even though you have a higher concentration of electrons in the N type semiconductor, they cannot diffuse into the P type semiconductor because there is a potential barrier. So, this diffusion is not possible.

Similarly, holes cannot diffuse into the N type semiconductor because of the barrier seen by the holes. So, we do not have any current. Now, when we apply a voltage, what happens? So, we will apply 2 types of voltages, the way we define them is forward bias. Forward bias when we say we mean the applied voltage is greater than 0. I applied positive voltage. When I do that, what would happen?

So, essentially my P type semiconductor has holes which you can think of as positive charge carriers. And we are applying a positive voltage to that. So, that would force these holes to move into the depletion region. Similarly, the negative terminal is connected to the entire semiconductor which will force the electrons to go into the depletion region. So, under forward bias the majority carriers diffuse into the depletion region.

Why does that happen? Even though there is a barrier the external voltage is actually forcing them to go into the depletion region. And there is a new equilibrium that is established. So, equilibrium is shift. So, what will happen? Essentially, the net space charge will reduce. Why

would it reduce? Because let us say electrons have moved into the depletion region from the N side.

So, there you have the space charges essentially from where the uncovered dopant atoms. Now, these electrons will go and get captured into the dopant atoms so that the charges you know are not there anymore. There are uncharged quasi neutral region it becomes. So, that is why as a majority carriers go into the depletion region, the space charge density reduces and then also the W depletion, the depletion width also reduces.

This is the effect of a forward bias. We can apply another type of bias which we call us reverse bias. So, V applied is less than 0. So, essentially, I am applying negative voltage to the P type and positive voltage to the N type. So, what happens now? Now, the majority carriers are coming out of the device. So, in this case here because we are applying a negative voltage when reverse in reverse bias holes will come out into the battery.

And then so electrons also would come out because a positive voltage will actually attract them. So, the in reverse bias, the majority carriers move out of PN junction device. So, what does that lead to? Well, you had this balance, where the electric field was exactly countering the electric field is countering the diffusion. So, you have excess of holes and electrons on either side and the diffusion is being countered with electric field.

But now, there is this additional battery which is actually helping to remove the majority carriers. So, that is why that the equilibrium shifts again. And now the net space charge density, charge increases and then W depletion which is the depletion width also increases. Why does that happen? Think about it this way. Let us say an electron has to come out here. Then essentially, it will shift eventually what will happen is you have an additional positive charge here.

So, the electrons have moved out into the external circuit. Similarly, on the P side, we will have additional negative charge. So, the space charge region has increased in the reverse bias. So, this is a fundamental principle in the operation of PN junctions. You might have already studied this in some form already. So, now, we want to go a little bit further than what we have seen.

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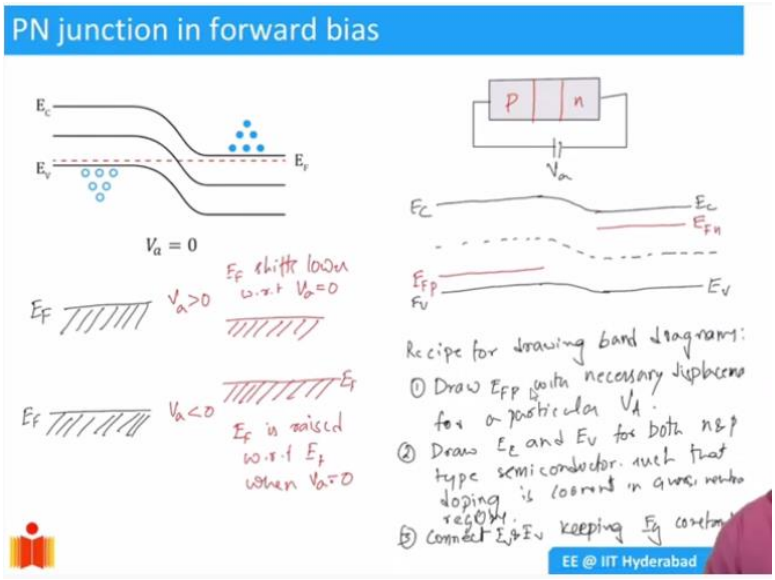


So, we want to understand this in terms of the energy band diagrams. So, we have already seen the equilibrium energy band diagram at no applied voltage. Now, what happens to the energy band diagram when you apply a voltage? So, what we are essentially doing is we are taking a PN junction and then we are biasing it. So, when the positive voltage positive terminal is connected to the P type semiconductor, what happens?

To understand that, we need to analyze what happens to a semiconductor in you know when you apply a potential. Let us say we under if you take a regular piece of semiconductor, it has basically lot of electrons and the level energy level at which the probability of finding electrons is half is given by $E_F$. So, this is essentially something similar to what you will you know you can take an analogy of water in a tank.

You can think of the water as electrons. And you have this lot of electrons in the tank, and the top surface of the water is like the Fermi level. Now, when I apply a positive voltage to this semiconductor, I am going to take out some electrons from the know the semiconductor. So, semiconductor can be thought of as a you know tank of electrons, and then you are taking out some of the electrons. So, what would happen?

The level of electrons would reduce similar to what happens in a tank. Here, if you take out some water, what you will have is little less water so the top level will move down. So, when you apply a positive voltage to a semiconductor, the Fermi level shifts lower. Basically, $E_F$ shifts lower with respect to $V_a$ equal to 0. When you compare with you know no applied voltage and applied voltage, the $E_F$ in the semiconductor will be lower.

What happens in the opposite scenario when there is a negative voltage? So, if you have negative voltage, let us say you have the energy originally like this $E_F$ is here. Now, we will apply a negative voltage $V_a$ less than 0. How would the Fermi level move? Now, in this case, we are actually having negative potential. So you are essentially adding more of electrons into the tank or more of electrons more of water into the tank. So, $E_F$ will move up.

So, in this case, the Fermi level will move up. So, $E_F$ is here now. So, basically, in this case, $E_F$ is raised with respect to $E_F$ when $V_a$ equal to 0. So, what essentially is happening is we are able to change the Fermi level up and down. And, why is this reasonable? It is reasonable because I mean conducting an connecting an external battery is essentially equivalent to taking out charges or putting in charges.

So, this is okay. So, now, what happens to the band diagram? So, we have previously seen a recipe to draw band diagrams. We will give you an equivalent recipe now. We will start with the Fermi level like in the previous case. So, if you have no applied voltage, we said the Fermi level has to be uniform all across the semiconductor. That was the Step 1. But now, we are applying a potential with respect to let us say, you know, potential is always applied with respect to something.

So, let us take the potential applied on the P type semiconductor related to the N type semiconductor. So, we will use N type semiconductor as a reference. Let us say I will put my $E_F$ here in the N type semiconductor. And, I have applied a positive voltage to the P type semiconductor related to the N type. So, my $E_F$ has to go lower. So, first, draw this correctly, this is the first step in the recipe. So, draw the Fermi levels.

So, you can even write out the recipe, recipe for drawing band diagrams. What is it? Step 1, draw $E_{FP}$ with necessary displacement for a particular applied voltage particular $V_A$. If you applied a negative voltage to the P type semiconductor then the $E_F$ has to go higher related to the N type $E_F$ that same correction. So, this is the first step in the recipe. The second step is draw $E_C$ and $E_V$ for both semiconductors both N and P type semiconductor such that doping is correct in quasi neutral region.

So, essentially if you are having a N type semiconductor, your $E_C$ has to be closer to $E_F$. So, $E_C$ will be somewhere here. Sorry, I will back. So, $E_C$ will be here. And similarly, let us say some appropriate distance. This will be $E_V$ and this will be $E_C$. What will happen to the P type semiconductor? Well, in this case, $E_V$ has to be here. And then at a certain level $E_C$.

This is $E_C$, $E_V$. So, we have drawn this. So, the $E_g$ is same. You know just because you have applied the voltage the $E_g$ is not going to change. So, the third step in the recipe was connect $E_C$ and $E_V$ keeping $E_g$ constant. This is the third step. So, I mean, we know from our understanding of electrostatics that there is a linear electric field. So, potential is going to be quadratic. So, it is going to be a quadratic shape, not a line, straight line.

So, this is it, essentially. And you can also draw the $E_I$ which is exactly middle. This is the band diagram of a PN junction with applied voltage. So, I will try to move this up slightly. So, this is my band diagram. I am not able to move it. So, this is how we draw band diagram.

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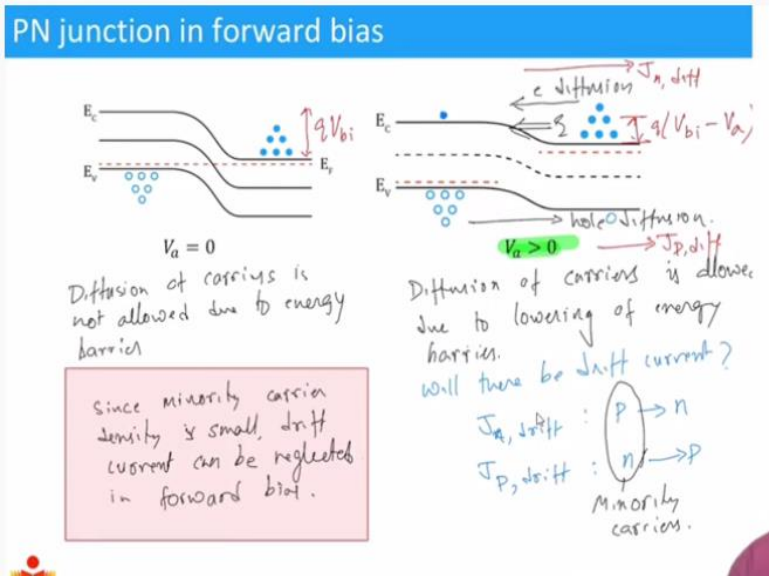


Now, we can quickly understand what happens in the forward bias. The same thing in a slightly better way it is definitely much better than my diagram but essentially same thing with additional electrons and holes shown here. This is for voltage which is positive. Now, what happens when you have such a scenario? When you had no applied bias, we said that there was no diffusion possible.

So, in the when applied voltage was 0, diffusion of carriers is not allowed due to energy barrier. Now, what happens when I have an applied voltage? The barrier has reduced you see here the

barrier now is only this much. In the previous case, it was a whole $qV_{bi}$. But now it is $q(V_{bi}-V_a)$. If applied voltage is positive, the barrier is lower. That is what we saw.

So, now, because of this you have this electrons in the N side which can diffuse into the P type. So, electron diffusion and similarly, you have the whole switch can diffuse. So, essentially, what is happening is diffusion of carriers is allowed due to lowering of energy barrier. So, essentially, we have current. So, what is the direction of current? Well, that is interesting.

So, if you have electrons which are flowing in the right to left, you have current. By convention, this should be $J_{n,diff}$. It is going in a positive direction. Similarly, holes are traveling in the you know positive direction. Holes are also current diffusion current for holes also is from left to right. Now, we want to ask a question. Will there be drift current?

Remember the basic difference between drift and diffusion currents. Diffusion current happens when you have a gradient in the concentration. Drift current happens when you have an electric field. The question here is, is there any electric field? Well, yeah, there is an electric field which is here. We know this. Yesterday did in detail last week. So, there is this electric field. So, electrons can actually go from P to N type.

So, when you have this, you can have a drift current consisting of $J_{n,drift}$ consisting of electrons which will go from P to electrons will go from P to n. But where are the electrons in the P type semiconductor? Well, they are there. We did not show in this picture. I have only shown holes here but then in principle they should be minority carriers which are electrons in the P type semiconductor. Similarly, they should be holes in the N type semiconductor.

So, there are this lesser number of carriers. But they are still there. So, similarly you can have $J_{p,drift}$ which is the drift of holes which will happen from n to P. So, this is essentially minority carriers. So, since minority carrier density is small, drift current can be neglected in forward bias. So, this is something that we need to keep in mind when we are analyzing. In the reverse bias, we will see that drift current is important. But in the forward bias we can neglect it.

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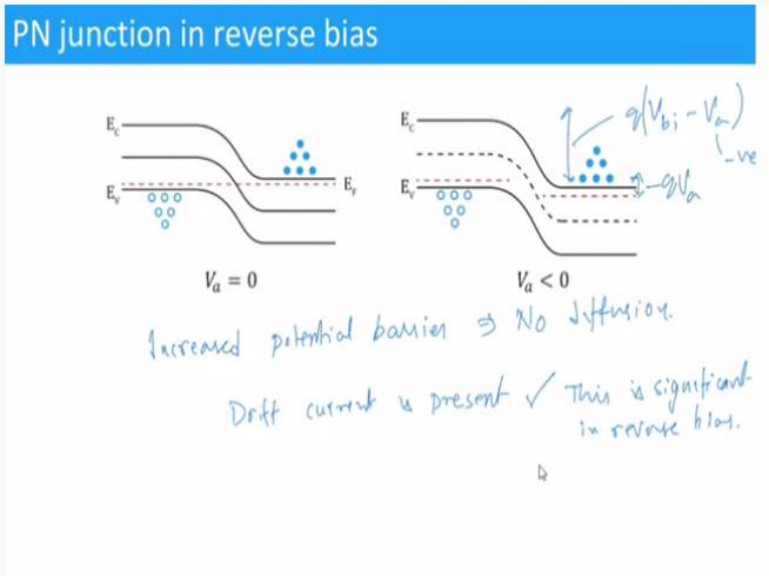


So, the same analysis we can do for the reverse bias as well. So, in the case of reverse bias, if you carefully work out this, you see that the Fermi level has now Fermi level of the P type semiconductor has moved slightly up. This is $q(V_{bi}-V_a)$, but now $V_a$ is negative. So, the whole thing is basically slightly shifted up the barrier. So, this difference in Fermi level is simply $qV_a$.

And this is your $q(V_{bi}-V_a)$. Since $V_a$ is negative, the whole barrier has increased in height. So, if barrier has increased in height, no diffusion. So, increased energy barrier increased potential barrier, both are same actually, barrier implies no diffusion. So, you essentially have some drift current. Drift current is present. And this is significant now, because you know the dominant contribution is not that this is the most important.

So, this is significant so in reverse bias. So, essentially we have the same sought of a band diagrams. You know, I would really strongly urge you to draw practice this band diagrams. Make sure that you follow the recipe. And you get exactly the same you know details because if you are able to draw the band diagram correctly, you understand quite a bit of your the physics.

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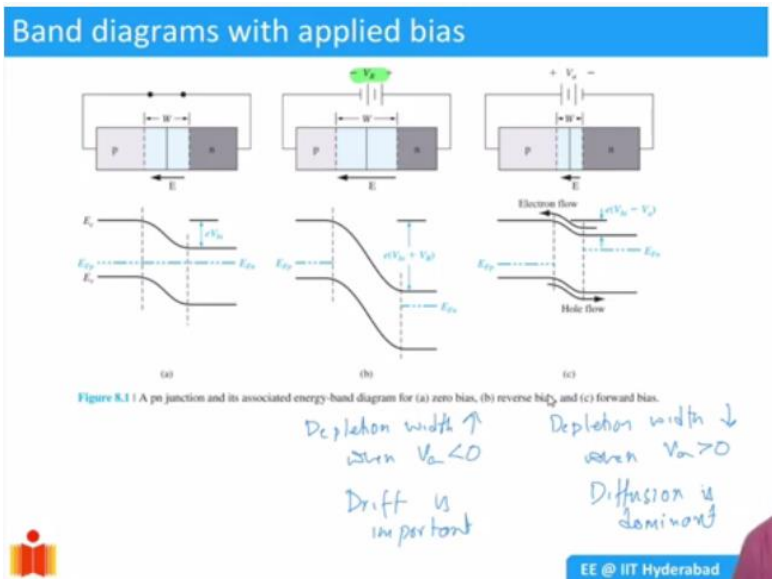


So, just you know, I wanted to summarize these aspects. Well, what you see here is that so you have the forward bias sorry without applied the same thing we have discussed. So, without any applied bias, you have the Fermi level which is constant. You know this is equilibrium PN junction. But the moment you are introducing applied voltage, if you apply let us say in this case is reverse bias.

So, you apply reverse bias, we are essentially increasing the energy barrier. And there is no flow of no diffusion of carriers. And you see that. So, basically here depletion width increases in reverse bias when $V_a$ is less than 0. And depletion width reduces when $V_a$ is greater than 0. This is forward bias. So, you can see that the barrier reduces. And essentially the space charge.

If your space charge region is larger, it is going to have a stronger I mean you it is going to have a you know electric field which is spread over a longer distance and hence more potential. So, it is kind of related to each other. So, the barrier is reducing, so you have a more easy flow of current. So, in the case of a forward bias, you have diffusion which is dominant. Here, drift is important.

It is not that there is no drift current in the forward bias. There is still there, but it is negligible compared to the majority carrier, you know, diffusion. So, essentially, this is a basic qualitative understanding of PN junctions. In the next video, we will essentially talk about the quantitative aspects. And to do that, we need to understand how the minority carriers are responding.

For example, here, you are taking holes from the P type semiconductor and then introducing them into the depletion region. And effectively some of these holes are going to reach into the N type semiconductor. So, they become minority carriers. So, we are introducing excess minority carriers into the N type and excess electrons into the P type. So, we will have to study how the minority carrier distribution changes.

And that will give you the current. So, in the next lecture, we will take some time and derive the expressions for minority carrier distributions. And we will also see how they are represented on the bands. So, with that, I would like to stop this video. We will see you in the next video, thank you.