Digital System Design
Professor Neeraj Goel
Department of Computer Science Engineering
Indian Institute of Technology, Ropar
Introduction to ASIC design flow Part - 2

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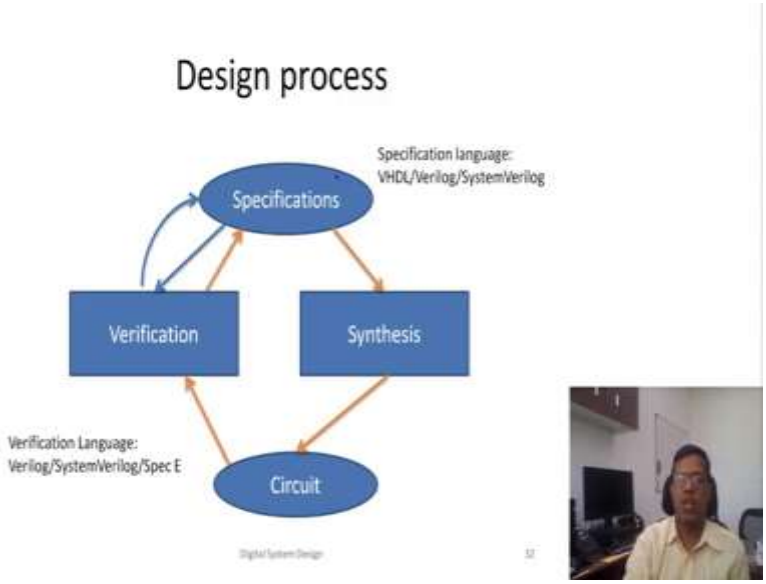

Now, with this background of standard cell now let us quickly look at the design process, this diagram we have seen earlier also. So, it starts with specification then we do synthesis then the circuit is a circuit in form gate is generated and in parallel we also do verification. So, and this iteration step would be there that if verification is not complete then or circuit is not correct then we will again go and change the specification.

So, the specification language could be a high level language like VHDL verilog, system very verilog and verification is also done using some specific languages like verilog using in our assignments for verification but system verilog and spec E are also other languages which can be used for verification.

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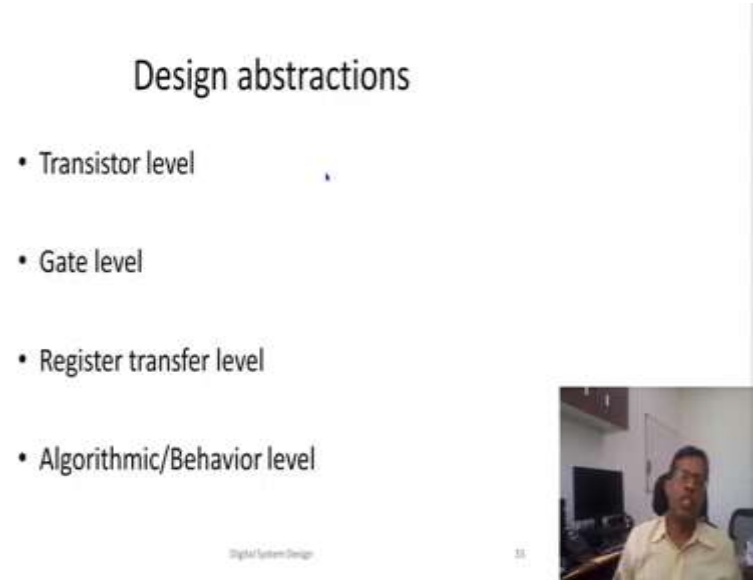

Now, if we have to design at for VLSI which has large-scale integration which may have a hundreds of thousands of transistors or millions of billions of transistors, then the only way we can design such a huge design is by divide and conquer or by using abstraction, by using hierarchy.

So, the abstraction level detail, so we can start with algorithmic level or behavior level then we have to go for register transfer level and then register transfer level will go for a gate level and then for each gate we can design a transistor which is coming from the standard cell library.

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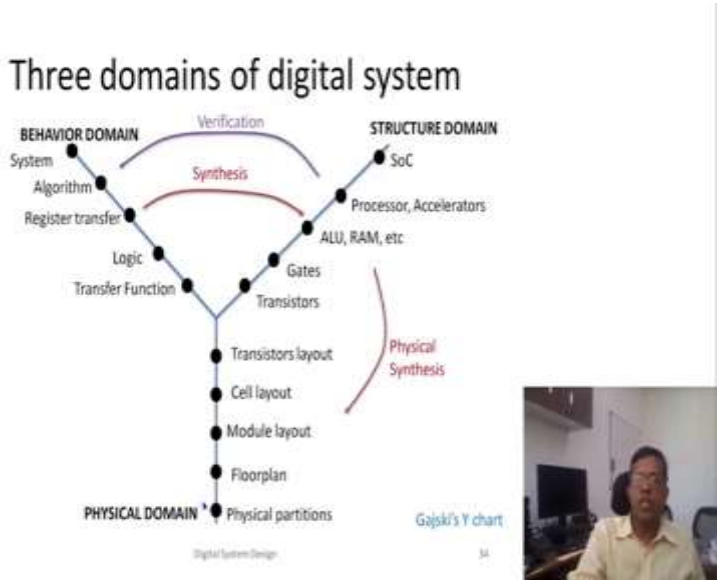

So, this design abstraction as well as for designing a whole complete chip the whole process can also be represented using this Y chart which is also called Gajski's Y chart, it represents three different domains of a design, behavior domain where we are talking about functions functionality or behavior of the application which we would like to generate an ASIC.

And then we would like to convert them into gates ALUs and their connections, etc that is all called structural domain and then finally a physical domain where layout is generated. So, what is a layout, basically a transistor will know that how many, where oxide has to be deposited where gate has to be deposited and where p and n concentrations would be there, so that is a transistor layout and using the standard cell library we also will get to know what is the cell layout, each layout of the each gate.

And then we can combine these layout of the gates to design our module layout and then floor plan and the whole physical chip. So, now when input specification is there the input or basically what we would like to design is usually an application, application essentially means it is a behavior, it is a functionality.

So, that functionality has to be converted into final structure in form of basic gates and these gates could also be hierarchically combined into larger blocks like ALU or memory or multiplexers, etc and these further could be combined into processors or accelerators or a group of these or maybe we can call them modules.

So, this behavior going from behavior to structure is called synthesis, so we have talked about it yesterday also in the previous lecture also, in the previous lecture we have seen that the behavior from after synthesis we will get a list of gates and how they are connected, this process is called synthesis.

Now, these gates could be further abstracted at different level of abstraction they can have could be grouped together in form of like ALU or RAM or multiplexers or adders, etc but they still finally we will have a gate level information. Now, at from the structure level also we would like to verify so that is also a verification step which always go in parallel with the synthesis step.

And yes, the next step from the so after this whole process of synthesis and verification finally we will have all the list of gates and how they are connected and when these gates are mapped to standard cell library elements cells then we also know that which gate will be mapped to which transistor, which particular cell.

So, we finally know the transistors involved associated with each kit, but it is still at the structural level, in the physical level we will have layout information. So, you remember when we say planar IC, so integrated circuit is all the transistors are in the same plane. So, that means there is a physical location, in one plane there is going to be a physical location for each of the transistor. So, where all those transistors are laid out is called layout.

So, in the layout we know where all the transistors are there, how they are connected to each other. So, they would be connected using wires but all that connection, that information is there, this whole information that where transistors are there, how they are connected is called physical synthesis, this whole process could be determined using physical synthesis. Now, what would be the steps?

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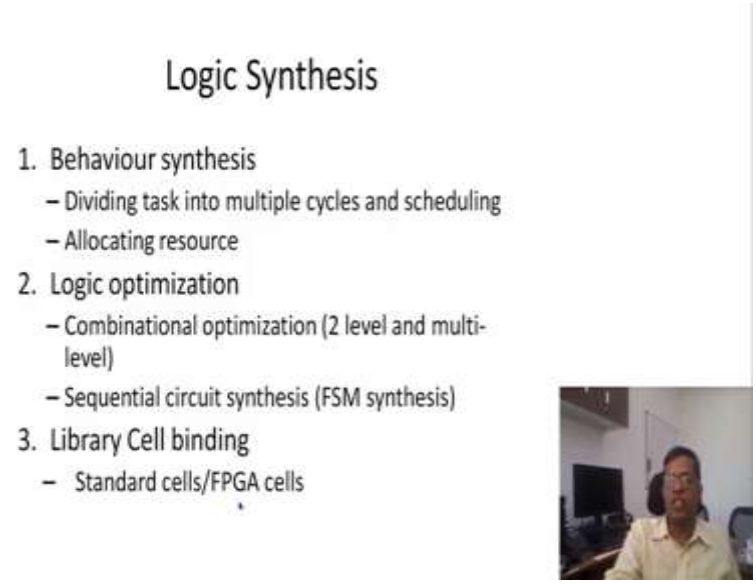

So, basically this is the replication of essentially previous lecture slide, so the first step is from the behavior to structure, so from behavioral structure we can call it logic synthesis or we can call it design synthesis. So, in design synthesis we can first step is behavior synthesis where we are allocating tasks to multiple cycles and scheduling, designing finite state machine, allocating resources.

And then the second step is logic optimization, logic synthesis. So, here from the behavior we get to know what logic is there that logic has to be optimized using two level and multiple level synthesis, multiple level optimization. So, here I would again categorically say that although in the, during the course we have focused more on two level synthesis but eventually multiple level synthesis would be automatically, the option see, the number of in the in the cell library, standard cell library we have seen the number of maximum number of input to a cell is a gate is four.

So, if more number of inputs are there automatically our two level circuit will also become multiple level circuits. So, that is why a multiple level combinational optimization for multiple level is more suitable and for that some sort of automation is required because that problem is sort of NP complete.

So, that logic optimization would be there and then after that we will also do FSM synthesis or sequential circuit synthesis. Finally all of that circuit would be bound to standard cell library so

which means that for each of the logic we will say that whether it will be mapped to two input AND gate or three input, so options are available every time.

And further we have to also see based on the objective whether the objective is low power or whether the objective is high performance or whether the objective is low area minimizing the area so we will see that various options of the cells are available for each functionality so based on the objective we can choose which options to be seen.

So, some of you have observed or have asked that now how we can limit so given a clock cycle how can we fit in more and more design into that. So, here if we take clock cycle as a constraint then sometime we have to take high performance cells, the cells which would result in the lowest latency could be selected. So, that is what would be in the purview of a library cell binding so that we can meet the objectives which are given as a as a design objective.

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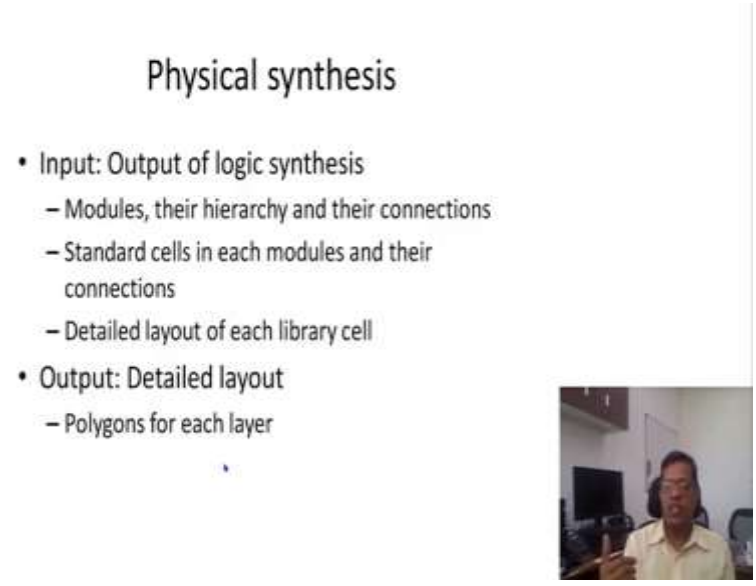

So, once this physical this logical synthesis is done that means we have the output of logic synthesis would be modules, their hierarchy connections standard cells of each module and their connections and detail layout of each cell is also there. So, that means overall we can say the output of my logic synthesis I know the layout of each library cell, I also know how many of them are there, which of them are there and how they are connected.

So, now I can take that as an input and finally I can lay out I can say the physical location of each and every cell and how they are connected, so that is what I would call detail layout so this will become the output. So, here not only the polygons for all the transistors but also how they are connected so each connection will also have their physical dimensions of the wire, that will all be included in the layout.

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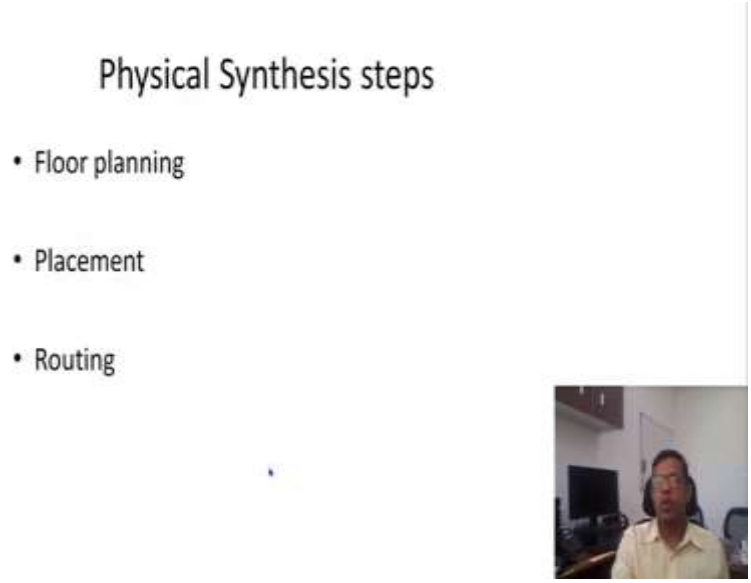

So, the steps usually followed in the physical layout are mostly can be categorized into three steps, one is floor planning, so that means overall dividing the area so you can assume it like this that if you are doing a city planning then you would allocate some area or maybe let us say campus planning you would allocate some area to the playground, some area to the hostels, some area to the academic block, some area to the residences.

And then each and every of this unit would be again further design you have to say that if it is a residences then how many flats would be there, where all these flats should be there, how roads should be connected so this is what is placement. And now, placement is essentially who will live where, so you will have let us say thousand students, these thousands which room would be allocated to which particular person.

So, let us say we would like to optimize you would say that each person should travel minimum, so that means you will say that the friends who are related to, so all the friends should try to stay nearby. So, this will give us the final placement where all the students who are related to each

other let us say one batch of the student who are all let us see in computer science or electrical they would live together so that would give them an option that they have to travel minimum, they will waste their minimum time in talking to each other, going to each other, so that is what is the overall placement objective that the delay for each of the or number of wires would be minimum.

And routing is essentially how the wires would be laid out so given the connections in the cells, in the gates how each of the wires so the problem with the routing is that two wires cannot cross each other, so if the two wires they have to be at certain distance so that they do not short each other, the effect of one should not reach the other wire, so that is why routing become a sophisticated problem in particularly in the planar ICs.

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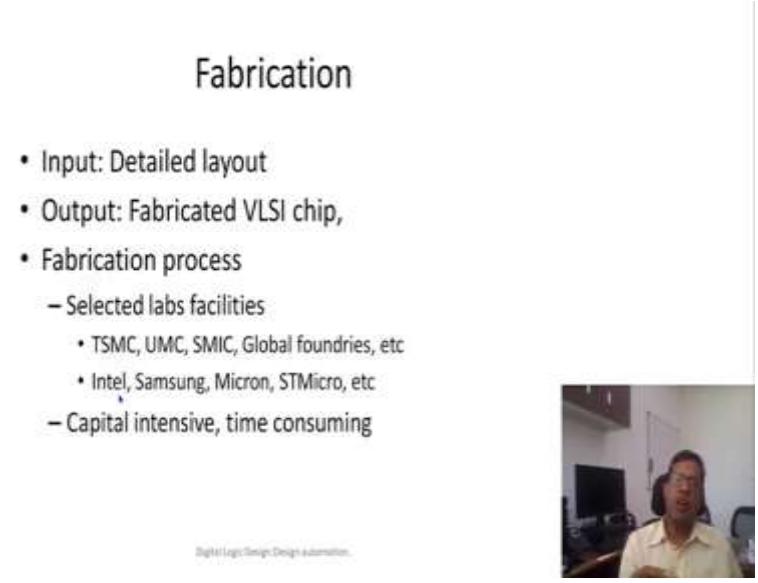

So, once all of these things are done then finally we will have a physical data, physical data of each and every layer, each and every metal layer or a transistor everything is that we can sum as a detailed layout. So, once this detail a layout is there then the next step will start which is a fabrication process.

So, once the layout is there then we have to fabricate the chip from the silicon, so this fabrication process is a very specialized process, it does not involve, it does not involve too much of understanding of digital design flow or even VLSI flow or about transistor so you need not to know all of those things.

So, but what should be known is a separately different science, it tends towards the manufacturing process, in the manufacturing process the layout is given, plan is given, now after the plan is given then you can go through the fabrication process so that is why what most of the companies are doing today they go, they will design up till the layout and after that only a couple of companies, two, three companies across the world they are fabricating for all the VLSI related companies.

So, the idea was started by some of the companies like NVIDIA, Qualcomm, Broadcom, so they were the initial fab less or fabrication they did not have any fabrication facility but today most of the companies even though they have their own fabrication facility they are sending it to some common lab fabrication facilities so that the cost could be minimized.

The common name which you can hear is TSMC which is in Taiwan state manufacturing company. So, UMC, SMIC is in China global countries in Europe so up there, these are the foundries which can take the fabrication data from anybody, even you as a individual can go ahead and send to these companies and then they can fabricate a chip to you.

On the other hand, there a couple of companies they are still fabricating their own chips so they have their own fabrication facilities like Intel, Samsung, Micron, ST microelectronics, Infineon, there are many of these companies they have their own fabrication facilities but yes since this whole fabrication process is hugely capital intensive like costly as well as the whole fabrication process is also time consuming.

Let us say you have designed something it will take 6 to 12 weeks so that your fabrication process is out and then you can take the chip so and then do the further processing. So, this fabrication process although an integrated part but still an isolated way because its input and output is clearly defined.

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Now, once this whole fabrication is done we have received the chip the next thing is before packaging people will first test it and they would have sophisticated tester so because you see the technology is at the scale of 20 nanometer to 45 nanometer, the size of the pin, input output pin would be very very small, so before putting those pins so the tester would try to give all those test patterns which you are usually giving in your verilog as a test bench so that tester will physically simulate, stimulate that 1.2 volt signal or 3.5 volt signal whatever is the input requirement and at this same interval whatever is required by the chip.

So, the testing is done, verification this is also called validation and testing at this moment and once it is verified that yes now chip is correct then people will pack it will package and once the it is packaged it will come in a ceramic board or ceramic package or a plastic package or different kind of packages are there so that they can minimize the heat.

So, and finally it would be placed onto a printed circuit board so that it could connect to other such chips. So, PCB designing would come even later so once a chip is designed. So, this is the overall process of ASIC design. So, in today's lecture we have talked about different components of the ASIC design and how given a specification how finally, final chip is fabricated so although we have talked about all of these things in quite brief you can go ahead and do other courses if you want to know more details.

So, but at this stage also it is important to know that whatever you have learned so far basically starting from gate design or a verilog design finally the whole process can be done even some because of the free pdk's you can and also their free EDA tools using those tools you can also design your own circuit till the stage of physical synthesis and the physical layout.

So, all those details are there and that can help you to go for a complete end-to-end chip design process. So, with this we would like to conclude the course, this is almost yeah. So, in the next part of this lecture we will talk about that what would be the future trends so what kind of things you can study if you want to know more about digital design. Thank you very much.