Digital System Design Professor Neeraj Goel Department of Computer Science Engineering Indian Institute of Technology, Ropar Introduction to ASIC design flow Part - 1

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Digital Design Flow for ASIC M6.03



Hello everyone, in our previous lecture we have discussed about a design flow for FPGA, today we are going to discuss about design flow for ASIC.

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Background - A few terms

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- Linear integrated circuit
 - All transistors on same plane
- Transistors: BJT, PMOS, NMOS, CMOS
- · ASIC Application specific integrated circuit

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- Integration levels
 - SSI (Small scale integration)
 - LSI (large scale integration)
 - VLSI (Very large scale integration)



So, let us first understand what is ASIC. To understand ASIC let us also go through couple of more terms, one important term is linear integrated circuit or we also call it IC integrated circuit and linear integrated circuit. So, basically integrated circuit is when number of transistors or your whole circuit is integrated onto one chip and this is specifically called linear integrated circuit because all the transistors, all the basic component of our circuit are laid out onto the same plane.

So, when you say one plane it is a 2D plane where all the transistors are placed at different positions so this is called linear integrated circuit. And what is a transistor? Transistor is a device which has usually three inputs. For example, if you see the other passive elements like registers, inductor, capacitor all of them had two inputs but transistor used to have three inputs so the earlier transistors were, so you would have heard of these names BJT bipolar junction transistor, PMOS or it is also called sometime simple MOS, PMOS, NMOS so and also CMOS, CMOS will have both PMOS as well as NMOS, it is a design method not but still it is called transistor.

So, if any transistor will have both the components PMOS as well as NMOS then it is called CMOS, CMOS is complementary MOS. So, now these are the various type of transistors which has been invented or which has been designed in last couple of years, last 40, 50 years but today most of the designs are usually focused on to the CMOS type of transistors which has both PMOS as well as NMOS, specifically in the digital design domain.

So, there is another term which is ASIC which we have said in the starting of this lecture ASIC is application specific integrated circuit. So, an integrated circuit which we are designing for a particular application, you can also say a circuit which is designed, being designed for a particular application is ASIC.

Now, by circuit here usually it means that it is a digital circuit, a digital circuit which is designed for a particular application is called an ASIC. You also see this word integrated here, integrated means how many transistors are put onto one particular chip that is the that also defines the scale of integration.

So, in small scale integration SSI circuits these number of transistors could be in the order of thousands and less than thousands and in a large scale integration when number of transistors grows beyond thousands and when the number of transistors will be in the range of hundreds of thousand then it will become VLSI very large scale integration.

So, when you say you will hear some of the related terms like VLSI design so that means a design which would have large scale integration involved, so that means we are focusing on a design which would eventually have more than thousands of transistors or hundreds of thousands of transistors.

So, when we started this course we talked about Morse law, so because of this Morse law because of this integration, increase in integration or increasing number of transistors per chip it has gone beyond hundreds of thousand limits. So, right now we have hundreds of million transistors or some of the chip also have more than a billion transistors on one integrated circuit or one chip.

So, that you can also call it very ultra large scale or very very large scale, you can coin all those words but they become meaningless because VLSI itself means it is going to be very large scale, it is the scale is beyond the limit of our hand crafted design. So, VLSI also mean that there has to be some sort of automation which should be there so that the number of transistors could be fitted in on to chip and could be designed. So, in today's lecture we will briefly go through this process of automation so that VLSI design could be feasible particularly the digital design.

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From Gates to Transistors

- Gates are designed by custom design engineers
- · Assumption for digital design
 - Standard cell library as input
- Standard cell library
 - Gates are called cells
 - Electric characterization: Average delay, area, power, capacitance, etc.
 - Physical characterization: Detailed layout, details about each layer

Digitalizer: Design Automation



So, now when we have seen in this particular course we were talking only and only about the gates not the transistors, we were talking about basic gates like AND gate, OR gate and NOT gate and we also talked about universal gates like NAND gate and NOR gate and then we have

also designed various blocks which were including which were designed using these gates and then those could be utilized to design something else.

So, for example, we have predominantly used multiplexers or flip flops and using multiplexers flip flop and adders we have designed further more sophisticated circuits. So, but we have not talked about transistors so who will design the transistor that is a one question which will come in our mind that who will design the transistor so that our digital design could be successful.

So, the answer to this question is usually it is designed by custom design engineers or analog design engineers not the digital design engineers, we assume that in our digital design we assume that these gates are available to us, somebody has designed it. So, when somebody has designed so possibly they have designed it and they have created a sort of library and this library is taken or assumed as a input.

So, what would be there in that library? See in that library there could be you can also say there could be only one gate universal NAND gate but no because of we would like to optimize our design for area sometime we would like to optimize our design for performance or power because of that various variants of each and every gate would be there.

For example, if there is a NAND gate there would be a different design for two input NAND gate, three input NAND gate, four input NAND gate. And similarly, for and OR gates also there will be multiple designs further because it is going to be designed by custom design engineers and analog design engineers, they will also think about what would be the load.

So, basically one output of the gate if it is going to multiple different gates then the it should be able to take care of the load capacitance, it should be able to take care of the fan out capacitance or fan out effect of fan out. So, to take care of the effect of fan out or design of the gate also need to be modified so that it can still be high performance.

So, sometime multiple variants of the gates would be designed based on the circumstance that if it is to be used for used in a case of high fan out then there would be internal design would be different, slightly different. So, when the standard, so this is called standard cell library, standard cells, what is standard here? So, internally there is some physical dimensions like height of the gate, physical height of the gate is fixed that is why it is called standard cell. So, if the standard cell library is the input so basically what do we mean when we say standard cell library is the input so it means that whenever digital design would take place some of the estimation has to take place.

Yesterday we have talked about that after placement and routing we clearly know what is going to be the delay, what is going to be the effect on the latencies, etc. So, all those latencies will come because the standard cell libraries are assumed as a input and because they are assumed as an input so there is some characterization which is involved.

So, for example, electrical characterization which means that for a particular gate what is the average delay. Characterization will also involve it will clearly tell what is the delay when output will go from high to low, what would be the delay when output will go from low to high.

Similarly, what would be the power consumption in each and every case, what is going to be the area, what is going to be the output capacitance, tray capacitance, all those electrical details are present to us in some abstracted manner so that whenever we analyze using the standard cell library, using this particular assuming this input then we can have some estimation that what is going to be the overall latency or what is going to be the minimum or maximum latency for our design.

So, that we can calculate a clock period, so that we can say that in one clock period how much design could be fit in. So, all those information is required so that we can choose, so that we, so that we can design our final circuit. So, this is the detail which is required electrical characterization is the detail which is required at so that we can design at our gate level.

But to move forward the physical characterization, physical detail is also required that what is the layout and what are the details about each and every layer. So, what are these layers, layout, etcetera we will talk in couple of minutes.

Standard cell library example

- · Free/open source standard cell libraries
 - Tanner, VTVT, IIT, OSU
 - Usually at older technologies
- Cadence, Synopsys, Mentor graphics
 - Free PDK



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So, also take some example of standard cell library, so yeah before that I will tell you that there is a couple of libraries standard celebrities which are present so some of them are free and open source, all these libraries also depends on that which technology we are working in so you these technologies refer to the fabrication technology, so you might have heard that 20 nanometer, 45 nanometer or 90 nanometer so these are all fabrication technologies, lower technology means more transistors could fit in.

And it also means that a lower technology node, basically the latest technology node, let us say 22 nanometer or 14 nanometer, it would have lesser delay, it would also consume lesser power

so and it would also be able to integrate more number of transistors per mm square or per area, per unit area.

So, earlier like 20 years back there were many free and open source technology libraries like tanner, VTVT, or Illinois, Institute of Technology have published their own open source library, OSU is another university which has published their own open source libraries so the very various open source standard cell libraries that has been published over internet and we can access them and the access is required so that we can have a complete design flow for digital design.

But the challenge with most of these technologies, most of these open source libraries were that they are usually designed in for older technologies like 180 nanometer or 350 nanometer so basically they were at the micron level. But today we have moved on to the latest technology which is 14 nanometer, 22 nanometer or 45 nanometers.

So, for the latest technologies we can still use the libraries which has been published by commercial companies like Cadence, Synopsys and Mentor graphics. So, these are the three major companies in electronics design automation field so which provide most of the software which is required for design automation.

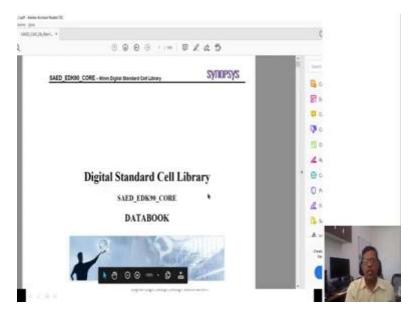
So, what they, they do not give open source but they give a free pdk, pdk is process development kit so this is still tied to a particular development node like 45 nanometer or 22 nanometer so or 90 nanometer and then it is free in the sense that they provide all the characterization information. For example, all these information so that we can use them in our design and we can design our digital design or ASIC based on these libraries.

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So, to give you some more detail I will share one of the document which shares the detail of this library.

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2	Inverting Buffer	IBUFFX32
3	Non-inverting Buffer	NBUFFX2
4	Non-inverting Buffer	NBUFFX4
5	Non-inverting Buffer	NBUFFX8
6	Non-inverting Buffer	NBUFFX16
7	Non-inverting Buffer	NBUFFX32
18	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX1

So, this is a digital standard cell library from the synopsis, it is for a 90 nanometer edk. So, when we see the detail so couple of things I would like to show in this detail. So, one thing I would like to show is the type of standard cells available. So, you see there are some six or seven type of inverters which are present, you see there are some six or seven type of inverters which are present.

So, when they say inverter x0 so that means the load is the minimum, here it can take inverter x32 can take up to fan out of 32. So, similarly, known inverting, inverting buffers are there so these buffers would be able to take more load. So, similarly non-inverting buffers so which are just the, so let us say one particular cell would have one particular gate has multiple fan out, so then non-inverting buffer so that the signal will not change but it would act as a buffer, it would be able to take much more fan out.

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9	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX2
0	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX4
1	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX8
2	Tri-state Non-Inverting Buffer w/ High-Active Enable	TNBUFFX16
3	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX32
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28	AND 3-input	AND3X2
29	AND 3-input	AND3X4
30	AND 4-input	AND4X1
11	AND 4-input	AND4X2
2	AND 4-input	AND4X4
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No	Cell Description	Cell Name
60	NOR 4-input	NOR4X0
61	NOR 4-input	NOR4X1
2	XOR 2-input	XOR2X1
63	XOR 2-input	XOR2X2
64	XOR 3-input	XOR3X1
15	XOR 3-input	XOR3X2
66	XNOR 2-input	XNOR2X1
67	XNOR 2-input	XNOR2X2
68	XNOR 3-input	XNOR3X(1
9	XNOR 3-input	XNOR3X2
	Complex Logic Gates	
0	AND-OR 2/1	A021X1
١.	AND-OR 2/1	A021X2
2	AND-OR 2/2	A022X1

So, you see in the logic gate also there are two input AND gates with multiple load factors, three input NAND, two input AND gate, three input AND gate, four input AND gate. So, this is also one of the reason that during the course, during the course we were kind of advocating that if the input is more than four input it is going to detroit.

So, because in the standard cell libraries like this they also take at most four input then after that they will break it into multiple of the AND gate. So, let us say if we would like to design a nine input AND gate so it would be designed using a four input and then another four input and another four input, two input, so or maybe two levels of three input AND gate.

So, similarly NAND gates are there or NOR, NOR, XOR, and XNOR, so all of these gates are available as a basic gate.

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8	XNOR 3-input	XNOR3X1
89	XNOR 3-input	XNOR3X2
	Complex Logic Gates	
70	AND-OR 2/1	A021X1
71	AND-OR 2/1	A021X2
72	AND-OR 2/2	A022X1
73	AND-OR 2/2	A022X2
74	AND-OR 2/2/1	A0221X1
75	AND-OR 2/2/1	A0221X2
76	AND-OR 2/2/2	A0222X1
17	AND-OR 2/2/2	A0222X2
78	AND-OR-Invert 2/1	AO(21X1
79	AND-OR Invert 2/1	A0(21)(2
90	AND-OR-Invert 2/2	A0(22X1
81	AND-OR-Invert 2/2	AOI22X2
82	AND-OR-Invert 2/2/1	A0(221X1
83	AND-OR-Invert 2/2/1	A0(221)X2
34	AND-OR-Invert 2/2/2	A0/222X1
85	AND-OR-Invert 2/2/2	A0(222)/2
e.)	OR-AND 2/1	0A21X1
ile Ar		0A21X1
ine ke 19 Det ja	a - mhait (a 8 8 8 8 a := 8 4 5	
103	antwert (ac. + ⊕ ⊕ ⊕ ⊕ = = = ⊕ ≠ ⊄ Ѣ Multiplexer 2 to 1	0 MUX21X2
103	antwent: ant. • ⊕ ⊕ ⊕ ⊕ = · = · ⊕ ℓ α ⋽ Multiplexer 2 to 1 Multiplexer 4 to 1	0 MUX21X2 MUX41X1
103	antwest: ant. • ⊕ ⊕ ⊕ ⊕ = = = ⊕ ≵ & ⊅ Multiplexer 2 to 1 Multiplexer 4 to 1	0 MUX21X2
103	antwent: antwent: B ⊕ ⊕ ⊕ = = ⊕ ≠ ₫ ⊅ ₫ Ѣ Multiplexer 2 to 1 Multiplexer 4 to 1 Multiplexer 4 to 1 Decoders	0 MUX21X2 MUX41X1 MUX41X2
103 104 105	Multiplexer 2 to 1 Multiplexer 4 to 1 Decoders Decoder 2 to 4	0 MUX21X2 MUX41X1 MUX41X2 DEC24X1
103 104	Multiplexer 2 to 1 Multiplexer 4 to 1 Decoders Decoder 2 to 4 Decoder 2 to 4	0 MUX21X2 MUX41X1 MUX41X2
103 104 106 107	Multiplexer 2 to 1 Multiplexer 4 to 1 Decoder 2 to 4 Decoder 2 to 4 Adders and Subtractors	0 MUX21X2 MUX41X1 MUX41X2 DEC24X1 DEC24X2
103 104 105 106 107	Multiplexer 2 to 1 Multiplexer 2 to 1 Multiplexer 4 to 1 Multiplexer 4 to 1 Decoder 2 to 4 Decoder 2 to 4 Adders and Subtractors Haif Adder 1 bit	MUX21X2 MUX41X1 MUX41X2 DEC24X1 DEC24X2 HADDX1
103 104 105 106 107 108	Multiplexer 2 to 1 Multiplexer 2 to 1 Multiplexer 4 to 1 Multiplexer 4 to 1 Decoders Decoder 2 to 4 Decoder 2 to 4 Decoder 1 bt Half Adder 1 bt Half Adder 1 bt	MUX21X2 MUX41X1 MUX41X1 DEC24X1 DEC24X2 HADDX1 HADDX2
103 104 105 106 107 108 109 110	Multiplexer 2 to 1 Multiplexer 2 to 1 Multiplexer 4 to 1 Decoder 2 to 4 Decoder 2 to 4 Decoder 2 to 4 Decoder 2 to 4 Adders and Subtractors Haif Adder 1 bit Haif Adder 1 bit Full Adder 1 bit	MUX21X2 MUX41X1 MUX41X1 DEC24X1 DEC24X2 HADDX1 HADDX2 FADDX1
103 104 105 106 107 108	Multiplexer 2 to 1 Multiplexer 2 to 1 Multiplexer 4 to 1 Decoder 2 to 4 Decoder 2 to 4 Decoder 2 to 4 Decoder 2 to 4 Adders and Subtractors Half Adder 1 bit Full Adder 1 bit Full Adder 1 bit Full Adder 1 bit	MUX21X2 MUX41X1 MUX41X1 DEC24X1 DEC24X2 HADDX1 HADDX2
103 104 105 106 107 108 109 110	Autorian State St	0 MUX21X2 MUX41X1 MUX41X2 DEC24X1 DEC24X2 HADDX1 HADDX2 FADDX1 FADDX2
103 104 105 106 107 108 109 110 111	Autoria Contractors Multiplexer 2 to 1 Multiplexer 4 to 1 Decoders Decoder 2 to 4 Decoder 1 bt Half Adder 1 bt Full Adder 1 bt	0 MUX21X2 MUX41X1 DEC24X1 DEC24X2 HADDX1 HADDX2 FADDX1 FADDX1 FADDX1 FADDX1
103 104 105 106 107 108 109 110 111 111 112	Autiplexer 2 to 1 Multiplexer 2 to 1 Multiplexer 4 to 1 Decoders Decoder 2 to 4 Decoder 1 bt 4 Half Adder 1 bt Full Adder 1 bt Full Adder 1 bt DFIp-Flops Pos Edge DFF Pos Edge DFF	MUX21X2 MUX41X1 MUX41X1 DEC24X1 DEC24X2 HADDX1 HADDX2 FADDX1 FADDX1 FADDX1 FADDX1 FADDX2 DFFX1 DFFX2
103 104 105 106 107 108 109 110 111 111 112 113	Multiplexer 2 to 1 Multiplexer 2 to 1 Multiplexer 4 to 1 Multiplexer 4 to 1 Decoder 2 to 4 Decoder 2 to 4 Decoder 2 to 4 Decoder 2 to 4 Adders and Subtractors Half Adder 1 bit Half Adder 1 bit Full Adder 1 bit D Filo-Flops Pos Edge DFF Pos Edge DFF Pos Edge DFF Pos Edge DFF, wi Async Low-Active Set	MUX21X2 MUX41X1 MUX41X1 DEC24X1 DEC24X2 HADDX1 HADDX2 FADDX1 FADDX2 DFFX1 DFFX2 DFFASX1
103 104 105 106 107 108 109 110 111 112 113 114 115	Multiplexer 2 to 1 Multiplexer 4 to 1 Multiplexer 4 to 1 Multiplexer 4 to 1 Decoders Decoder 2 to 4 Decoder 2 to 4 Decoder 1 bt Half Adder 1 bt Half Adder 1 bt Full	MUX21X2 MUX41X1 MUX41X1 MUX41X2 DEC24X1 DEC24X2 HADDX1 HADDX2 FADX1 FADX1 FADX2 DFFX1 DFFX1 DFFX2 DFFX2
103 104 105 106 107 108 109 110 111 111 112 113 114	Multiplexer 2 to 1 Multiplexer 4 to 1 Multiplexer 4 to 1 Decoder 2 to 4 Decoder 2 to 4 Decoder 2 to 4 Adders and Subtractors Haif Adder 1 bit Haif Adder 1 bit Full	MUX21X2 MUX41X1 MUX41X1 MUX41X2 DEC24X1 DEC24X1 DEC24X2 HADDX1 HADDX2 FADDX1 FADDX1 FADDX2 FADDX1 FADDX2 DFFX1 DFFX2 DFFX2 DFFAX1
103 104 105 106 107 106 107 108 109 110 111 112 113 114 115 116 117	Multiplexer 2 to 1 Multiplexer 4 to 1 Multiplexer 4 to 1 Multiplexer 4 to 1 Decoders Decoder 2 to 4 Decoder 2 to 4 Decoder 1 bt Half Adder 1 bt Half Adder 1 bt Full	MUX21X2 MUX41X1 MUX41X1 MUX41X2 DEC24X1 DEC24X2 HADDX1 HADDX2 FADX1 FADX1 FADX2 DFFX1 DFFX1 DFFX2 DFFX2

Some of the complex gates are also available where AND and OR are there so basically it takes two input to the AND gate and one of the input as or gate so this is a combination, so this is, this will take two AND gate and two OR gate as input, so it is a combination of gates so that in certain cases we can optimize, directly optimize, directly map our circuit to these gates and these gates are going to be much more optimized than if we use one AND gate and one OR gate.

So, such complex gates are also available in the standard cell library which would help in the improvement of the performance. So, some of the small decoders, multiplexers, half adders are also there.

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e,a,	MC, 1	
	8 8 8 8 = = # # # # B	
21	Pos Edge DFF, w/ Sync Low-Active Set & Reset	DFFSSRX2
22	Neg Edge DFF	DEENX1
23	Neg Edge DFF	DFFNX2
24	Neg Edge DFF, w/ Async Low-Active Set	DFFNASX()
25	Neg Edge DFF, w/ Async Low-Active Set	DFFNASX2
26	Neg Edge DFF, w/ Async Low-Active Reset	DFFNARX1
27	Neg Edge DFF, w/ Async Low-Active Reset	DEFINARX2
28	Neg Edge DFF, w/ Async Low-Active Set & Reset	DEENASRX
29	Neg Edge DFF, w/ Async Low-Active Set & Reset	DFFNASR/(2
30	Neg Edge DFF, wi Async Low-Active Set & Reset, Only Q out	DFFNASRQX1
31	Neg Edge DFF, w/ Async Low-Active Set & Reset, Only Q out	DFFNASRQX2
32	Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out	DFFNASRNX1
33	Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out	DFFNASRNX2
	Scan D Flip-Flops	
34	Scan Pos Edge DFF	SDFFX1
35	Scan Pos Edge DFF	SDFFX2
36	Scan Pos Edge DFF w/ Async Low-Active Set	SDFFASX1
37	Scan Pos Edge DFF w/ Async Low-Active Set	SDFFASX2

95,8	MC 1	3
	8 9 9 8 = = 8 # # B	
11	Full Adder 1 bit	FADDX2
	D Flip-Flops	10.00
12	Pos Edge DFF	DFFX1
13	Pos Edge DFF	DFFX2
14	Pos Edge DFF, w/ Async Low-Active Set	DFFASX(1
15	Pos Edge DFF, w/ Async Low-Active Set	DFFASX2
16	Pos Edge DFF, w/ Async Low-Active Reset	DFFARX1
17	Pos Edge DFF, w/ Async Low-Active Reset	DFFARX2
18	Pos Edge DFF, w/ Async Low-Active Set & Reset	DFFASRX1
19	Pos Edge DFF, w/ Async Low-Active Set & Reset	DFFASRX2
20	Pos Edge DFF, w/ Sync Low-Active Set & Reset	DFFSSRX1
21	Pos Edge DFF, w/ Sync Low-Active Set & Reset	DFFSSRX2
22	Neg Edge DFF	DFFNX1
23	Neg Edge DFF	DFFNX2
24	Neg Edge DFF, w/ Async Low-Active Set	DFFNASX1
25	Neg Edge DFF, w/ Async Low-Active Set	DFFNASX2
26	Neg Edge DFF, wi Async Low-Active Reset	DFFNARX1
27	Neg Edge DFF, w/ Async Low-Active Reset	DFFNARX2
28	Neg Edge DFF, w/ Async 🎍 🕙 💿 🚥 🗠 😰 🚠	DFFNASRX1
20	Man Edus DEE withman Law Action Sat & Darot	DECKIA COVER

Neg Edge DFF, w/ Async Low-Active Reset DFF Neg Edge DFF, w/ Async Low-Active Reset DFF Neg Edge DFF, w/ Async Low-Active Set & Reset DFFN Neg Edge DFF, w/ Async Low-Active Set & Reset DFFN Neg Edge DFF, w/ Async Low-Active Set & Reset DFFN Neg Edge DFF, w/ Async Low-Active Set & Reset, Only Q out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only Q out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only Q out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only Q out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out DFFNA	FNARX2 NASRX1
Neg Edge DFF, wi Async Low-Active Reset DFF Neg Edge DFF, wi Async Low-Active Set & Reset DFFN Neg Edge DFF, wi Async Low-Active Set & Reset DFFN Neg Edge DFF, wi Async Low-Active Set & Reset, Only Q out DFFNA Neg Edge DFF, wi Async Low-Active Set & Reset, Only Q out DFFNA Neg Edge DFF, wi Async Low-Active Set & Reset, Only Q out DFFNA Neg Edge DFF, wi Async Low-Active Set & Reset, Only QN out DFFNA Neg Edge DFF, wi Async Low-Active Set & Reset, Only QN out DFFNA Neg Edge DFF, wi Async Low-Active Set & Reset, Only QN out DFFNA Scan D Filo-Flops DFFNA	NASRX1
Neg Edge DFF, wi Async Low-Active Set & Reset DFFN Neg Edge DFF, wi Async Low-Active Set & Reset DFFN Neg Edge DFF, wi Async Low-Active Set & Reset, Only Q out DFFNA Neg Edge DFF, wi Async Low-Active Set & Reset, Only Q out DFFNA Neg Edge DFF, wi Async Low-Active Set & Reset, Only Q out DFFNA Neg Edge DFF, wi Async Low-Active Set & Reset, Only QN out DFFNA Neg Edge DFF, wi Async Low-Active Set & Reset, Only QN out DFFNA Neg Edge DFF, wi Async Low-Active Set & Reset, Only QN out DFFNA Scan D Filo-Flops DFFNA	
Neg Edge DFF, w/ Async Low-Active Set & Reset DFFN Neg Edge DFF, w/ Async Low-Active Set & Reset, Only Q out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only Q out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only Q out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out DFFNA Scan D Filo-Flops DFFNA	NASRX1 NASRX2
Neg Edge DFF, w/ Async Low-Active Set & Reset, Only Q out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only Q out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out DFFNA Scan D Filo-Flops DFFNA	NASRX2
Neg Edge DFF, w/ Async Low-Active Set & Reset, Only Q out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out DFFNA Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out DFFNA Scan D Filo-Flops DFFNA	
Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out DFFN# Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out DFFN# Scan D File-Flops DFFN#	ASROX1
Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out DFFNA Scan D Filo-Flops	ASROX2
Scan D Filp-Flops	ASRNX1
CONSISTERNAL CO.	ASRNX2
Scan Pos Edge DFF	SDFFX1
Scan Pos Edge DFF 3	SDFFX2
Scan Pos Edge DFF w/ Async Low-Active Set SDI	DFFASX1
Scan Pos Edge DFF w/ Async Low-Active Set SD	OFFASX2
•	
SYNOPSYS ARMENIA Educational Department Rev. 1.4 Page 2	22 of 100

Now, you see only the D flip flop is present, you will not see JK flip flop, RS flip flow or T flip flop because, but D flip flop is present in almost different kind of variants like D flip flop with a synchronous reset set, with asynchronous reset set as well as reset, so these positive edge, similarly negative edge so all variants of D flip flops are present but not the other flip flops. Since, if we have D flip flow we can also convert, we can design other flip flops also. So, scan D flip flop is a very special type of D flip flop which is used for sequential purpose.

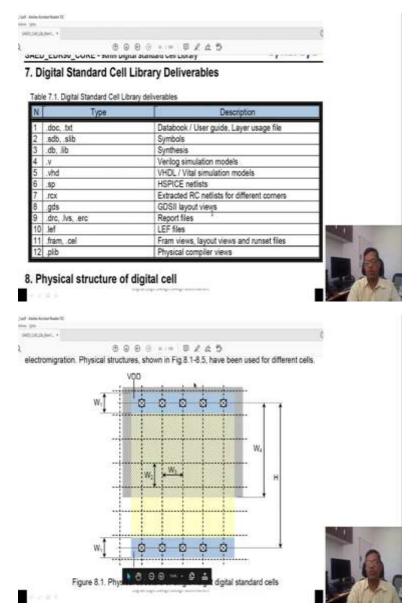
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51	ocali ivey cuye unn ili Asjilic cumActive nesel	JUTTIMALAL
52	Scan Neg Edge DFF w/ Async Low-Active Set & Reset	SDFFNASRX1
53	Scan Neg Edge DFF w/ Async Low-Active Set & Reset	SDFFNASRX2
	Latches	
54	RS NAND Latch	LNANDX1
55	RS NAND Latch	LNANDX2
56	High-Active Latch	LATCHX1
57	High-Active Latch	LATCH02
58	High-Active Latch w/ Async Low-Active Set	LASX1
59	High-Active Latch w/ Async Low-Active Set	LASX2
60	High-Active Latch w/ Async Low-Active Reset	LARX1
61	High-Active Latch #/ Async Low-Active Reset	LARX2
62	High-Active Latch w/ Async Low-Active Set & Reset	LASRX1
63	High-Active Latch w/ Async Low-Active Set & Reset	LASR//2
64	High-Active Latch w/ Async Low-Active Set & Reselvonly Q out	LASROX1
65	High-Active Latch w/ Async Low-Active Set & Reset only Q out	LASRQX2
66	High-Active Latch w/ Async Low-Active Set & Reset only QN out.	LASRNX1
67	High-Active Latch w/ Async Low-Active Set & Reset only QN out	LASRNX2
	Clocked Gates	
68	Clock Gating cell w/ Latched Pos Edge Control Post	OGLPPSX2

78 79 80	8883×≔ 8⊀		11
79 80		25	
79 80	Clock Gating cell w/ Latched Neg Edge Control Pre-		CGLNPRX2
80	Clock Gating cell w/ Latched Neg Edge Control Pre		CGLNPRX8
80	Delay Lines		00001100
	Non-inverting Delay Line, 250 ps		DELLN1X2
	Non-inverting Delay Line, 500 ps		DELLN2X2
82	Non-inverting Delay Line, 750 ps		DELLN3X2
	Pass Gates		
83	Pass Gate		PGX1
84	Pass Gate		PGX2
85	Pass Gate		PGX4
	Bi-directional Switches		
86	Bi-directional Switch w/ Low-Active Enable		BSLEX1
	Bi-directional Switch w/ Low-Active Enable		BSLEX2
	Bi-directional Switch w/ Low-Active Enable		BSLEX4
	Isolation Cells		
89	Hold 0 Isolation Cell (Logic AND)		ISOLANDX1
	Hold 0 Isolation Cell (Logic AND)		ISOLANDX2
	Hold 0 Isolation Cell (Logic AND)		ISOLANDX4
	Hold 0 Isolation Cell (Logic AND)		ISOLANDX8
	888 · · · · · · · · · · · · · · · · · ·	a D	
	High to Low Level Shifter/ Low-Active Enable		LSDNENX4
34	High to Low Level Shifter/ Low-Active Enable		LSUNENAS
	Retention Filp-Flops and scan Flip-Flops		000000
-	Pos Edge Retention DFF		RDFFX1
13			
13	1		

Now, different kind of latches, in latches we have RS NAND, RS NAND type latch. So, all of these other gates pass transistors delay lines so these are isolation gates these are for low power or different use cases. So, that was not the purpose.

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Now, the other thing which yeah, so once a digital standard cell library has been given as an input it also gives basically symbols, synthesis and verilog simulation models, HSPICE netlists, so all of these things are will come with the standard cell library, so it can help in the digital design so that we can estimate area, power, etcetera and we can also simulate the design.

And on the second side it can also help us in the physical compilation which we will talk about in couple of slides. So, physical compilation view is there, report files, GDSII layout view is there so that we can convert into layout also. So, yeah, so this is what is the meaning of physical layout that it means that if this is the overall cell that from the VDD so from the power supply to ground this is going to be the dimension, this is the width 1, width 2 and it is formed in the form of a great.