Introduction to Time – Varying Electrical Networks
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Lecture No. 68
LPTV networks with sampled outputs: Switched capacitor circuits

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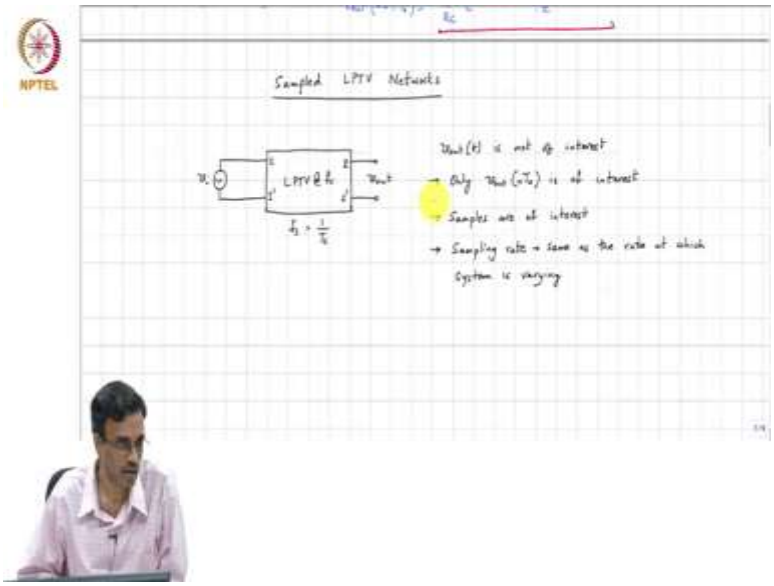

So, the next thing that I would like to talk about is basically sampled LPTV networks. It turns out that a very, very common application of LPTV networks or LPTV circuits is where the output so, this is the LPTV at fs, and let us say this is some voltage which is driving the LPTV network, and this is v out. What is a very common application is that the entire waveform v out of t is not of interest, only v out of n times ts is often interest.

In other words, it is the output samples that are of that are of interest, the complete waveform. So, samples are of interest and the entire waveform is not something that we worry about. And the other key thing is that the sampling rate is same as the rate at which the system is varying. So, that is the, these are the two key points to understand.

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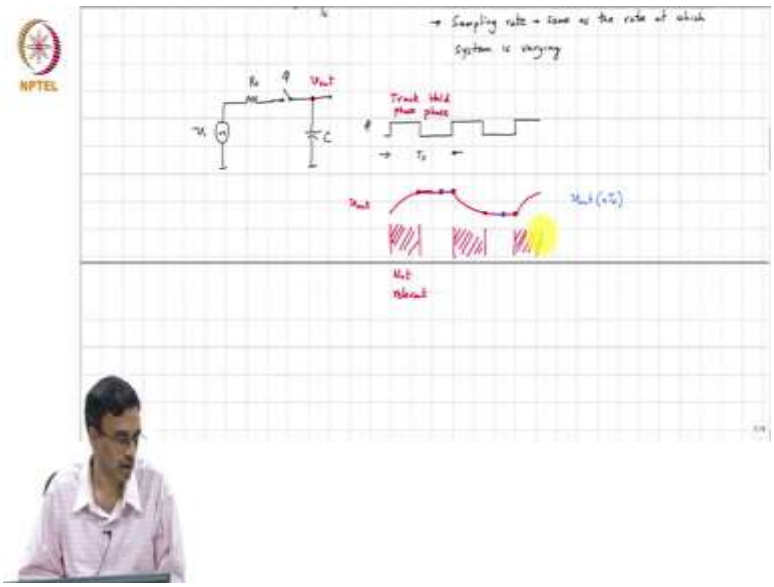

And the question is, where do these, why is this so important? And I can, I will discuss a few of the circuits that hopefully, will convince you that this is indeed samples are important in a whole lot of applications. So, let us say you were trying to build a sample and hold, the simplest form of sample and hold that you can think of or a track and hold is.

So, this is a clock and this is the capacitance and this the clock is, the switch is opened and closed periodically with a duty cycle of say 50 percent so this is ts. So, this is the period during which the switch is closed is called that track phase, and the period or the fraction of the period when the switch is open is called the hold phase.

And well, during the track phase, the input source is connected to the capacitor. And through the output impedance of the source or rs can also model the switch resistance, the capacitor attempts to charge towards vi. But of course, there will always be some voltage drop across a switch because there is some capacitor current flowing and that will cause a drop across the switch. And once the track phase is over and then you open the switch, the capacitor is voltage is held.

So, the representative waveform, output waveform is basically something like this. Now of course, it depends on the input waveform of course, but as you can see, this part is not relevant as far as the next stage is concerned. The next stage is only interested in the held value? In other words, it is interested in say the value of the capacitor voltage at, I mean, at any one of those points in the hold face. So, you can pick any one of those points as being your relevant points.

Similarly, so let us say that is the relevant point and similarly, this is the relevant point and so on. And so, therefore, it is these sampled values. So, v out of n times ts that are. So, this is a simplified example of a track and hold, which is a system where again where the output I mean, where only the samples are relevant.

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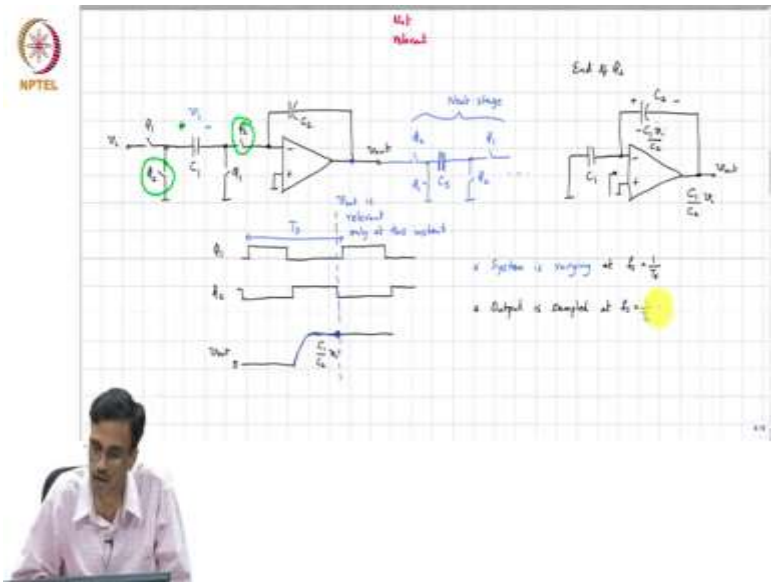

For those of you who have seen switched capacitor circuits in the past here is an example. So, if you have not seeing switch capacitor circuits, do not worry about it. So, this is an example of what is called a switched capacitor, integrator, the op amp of course, in reality is going to be have finite bandwidth and so on. And the way this works is the following.

So, phi 1 is a clock phase like this, phi 2, ph 1 is a clock phase like this, phi 2 is non-overlapping with phi 1 and as this. And phi 1a is almost the same as phi 1 or for the purposes of discourse I will just make phi 1a the same as phi 1. Those of you who have done switched capacitor circuits before you know why I need a slightly different phase there. But at least in theory, it can be the same as phi 1. So, during phi 1, the, these switches are off. These switches are off and the voltage across the capacitor is simply.

Student: V1

Professor: Is simply V1 or Vi. During phase two what happens? The capacitor c1, which was charged to Vi is connected to ground is connected to c2. So, what comment can we make about what will happen the capacitance, the op amp gain is infinite. And so, if you think of this as a

miller capacitor, the effective capacitors looking in is infinity. So, all the charge on this capacitor and c1 will go into c2. So, at the end of phase 2o the voltage, so this will all at the end of phase 2, this becomes 0, and this becomes. The voltage across that capacitance becomes c1.

The charging was, yea, so it was minus the voltage like that. The charge in this plate was minus c1 times Vi, so that is the charge on that plate now, and therefore, this becomes minus c1 Vi by c2 so the output voltage will be plus c1 by c2 times Vi. So, in reality of course, you know, the op amp has got some finite gain bandwidth. And if you look at the output, the output vout is going to be in our example is going to be 0 during phase 1 and phase 2, it is going to do something that depends on the details of the gainned bandwidth.

Of course, all of you know that the op amp is also nonlinear it can slue. And but eventually it settles and it will settle to a value of c1 by c2 times Vi and stays like that for the next half clock period. Now, this this is this is what is called a switch capacitor integrator. Now, the output of this integrator is going to be read or sensed by a similar switch capacitor circuit. So, this is the next stage. So, let us say this samples on phase 2, for instance. Anyways there is many ways to do this, but there is something representative here, and this goes.

So this is the next stage. So, what is happening? Well, the next stage is sampling the output of this first stage. And at what point I mean, and so what is the output or when is the output of the first stage relevant to the second stage?

Student: When the phi t is high after sometime.

Professor: So, basically the, this capacitor let us call this c3 is connected across the output of the op amp and is going to also have a waveform like this. So, at the end of phi 2 is when the charge on c3 is trapped, and it is processed by the next stage, correct. So, the sampling in when the time of interest is not or rather the waveform is not really interesting for us or for the next stage at any other time, it is only of interest at the falling edge of…

Student: Phi 2.

Professor: Phi 2. Does it make sense? And the period with which phi 1 an the phi 2 are changing they are all varying periodically with ts. So, this is another example of a system, which is varying periodically with time. And what is the period with which the system is varying? System, so if I

assume that that is ts is varying at fs which is 1 over ts, output is sampled at the same rate. Does it make sense?

Now a third example. I mean switch capacitor circuits are very, very useful in practice and are used in virtually all families of A to D converters. Latches are another example of linear periodically time varying system where you, you were looking at a continuous time input. And it is only the you sample the output at certain clock edge and make a decision on that on the sampled output at that point. So, the next.