Introduction to Time - Varying Electrical Networks
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Lecture 47
N-path example: Time-Interleaved ADCs

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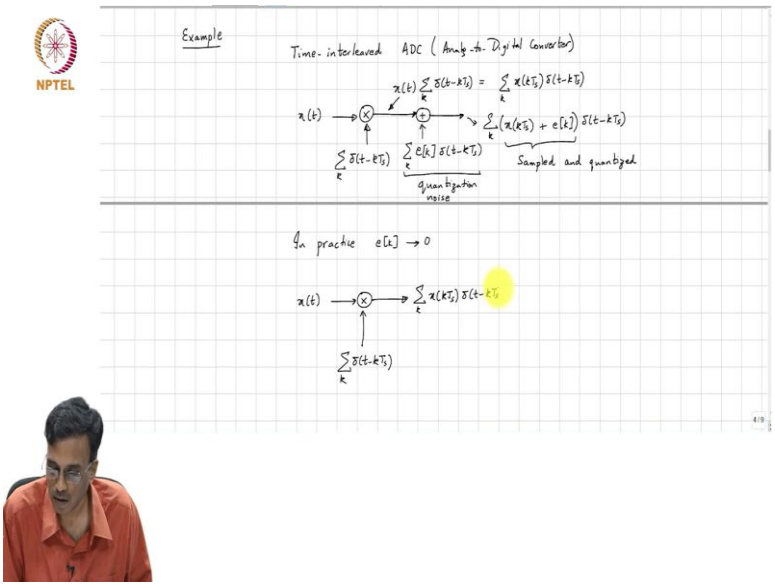

So, let us take a look at a practical example which uses this N-path principle to great advantage. And this is, there are many such systems and one of them is time interleaved ADC, those of you do not know what an ADC is this is an analogue to digital converter. So, the basic idea behind an A to D conversion is you take an input, you sample it and remember that from a signal processing point of view, let us say this is the input x of t, you multiply this by dirac delta train, delta of t minus k Ts.

So, the output is simply sigma over k, thank you, x of k Ts, delta of t minus kt. Of course, in the real world, I mean, there is no impulse functions and there is no delta train, but mathematically, this is what happens and then it turns out that there is quantization noise added. So, this is e of sigma over k, e of k delta t minus k Ts and this is quantization noise and so, that is this here and after sampling and quantization what you have at the output is x of k Ts plus e of k delta of t minus k Ts the sum over all k.

So, this is the sequence which is not only sampled and quantized. And of course, in practice e of k is so small that it tends to 0 or so small that it can, it should be chosen. So, that it can be so small as to be neglected in the system. So, for all practical purposes as far as signal processing equivalent of an A to D converter is concerned you can think of it as x of t sum over k or delta of t minus k Ts and consequently, this is k Ts.

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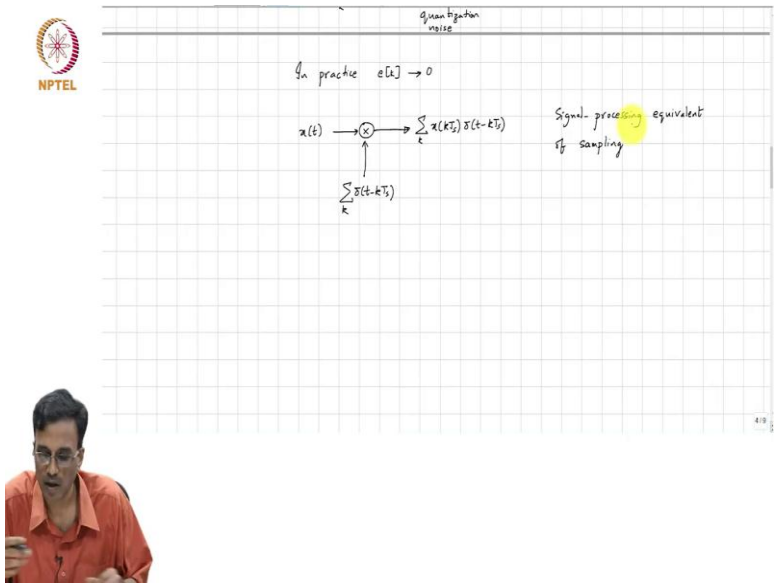

So, this is the signal processing equivalent of sampling. Now, unfortunately there is in practice you know if you want to sample wider and wider bandwidth, the sampling rate has to become higher and higher. And physically there is a limit on how fast you can sample. But there are many applications which needs sampling rates which are much higher than what is possible with a, in a given process technology.

For example, if you want to make a very high speed scope or if you want to make a converter in, which wants to digital signals coming in, in the across a link in a data centre, the rate at which you need to sample can be several tenths of Giga samples per second, which, therefore, which is may not be feasible to do efficiently. So, there is always, a need to be able to achieve A to D conversion at higher and higher speeds. And many times the speeds are at, the speeds can exceed the capability of a given technology.

So, now, the question is, well, then can we, how can we leverage the use of slower rate A to D converters? How can we combine them to make a box, which behaves like an A to D converter, that runs at a much higher speed, but where all the individual subsystems that are running at a much lower speed and one example of that, I mean, that basically is one embodiment of the N-path principle. And that is time interleaving.

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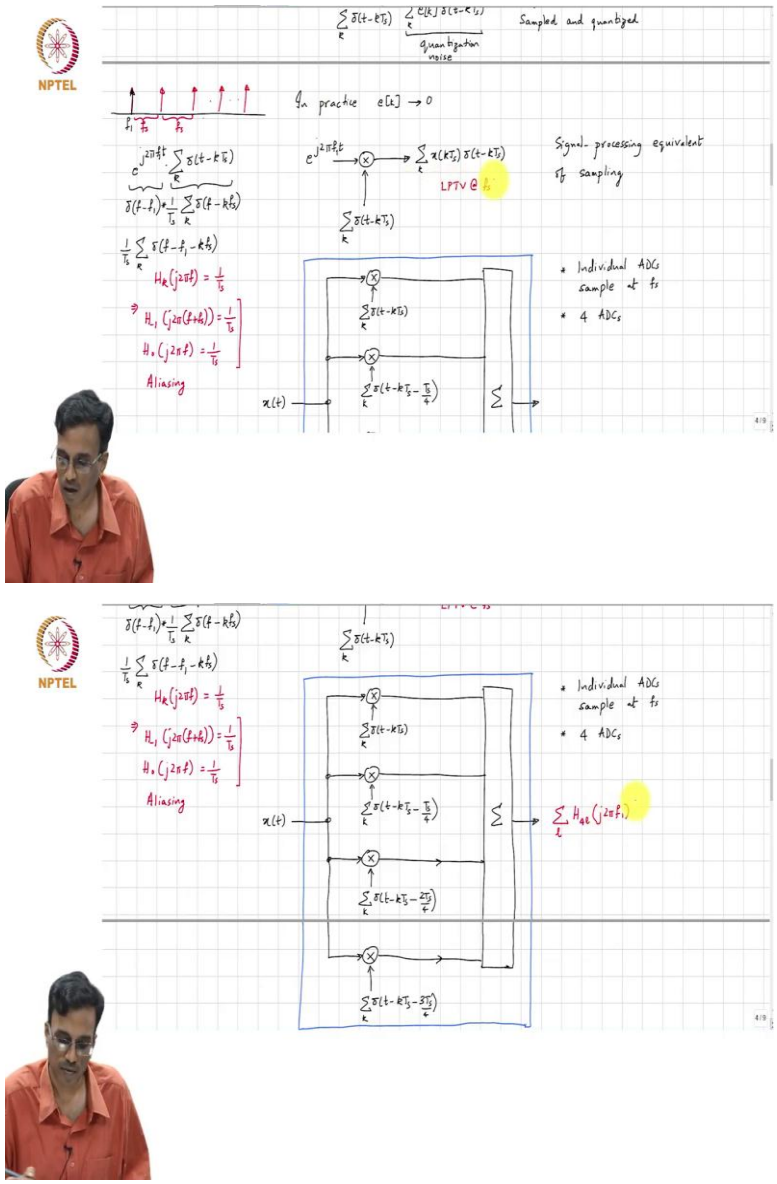

So, I am going to illustrate it with again, I am going to illustrate it with a number, with a small number let us say 4. So, you have 4 channels. So, this is the combined box and as you can see, the individual subsystems are all working at fs, 4 ADCs, and so, if you take and remember, that each ADC basically is multiplication by delta train. So, it is an example of a linear periodically time varying system and so when you multiply in the time domain, it is the same as convolution in the frequency domain.

So, if you look at, if you want to look at the spectrum of the output, you have to convolve the spectrum of this, which is an impulse function at, oh let us call this f 1, f minus f 1 and this is again a train of impulses, which is delta of f minus k times fs and the multiplication becomes

convolution here. So, this basically is 1 over Ts times sum over k delta of f minus f 1 minus k fs and so, therefore, you can see that all the harmonic transfer functions,.

So, if you draw a picture, if the input was at a frequency f1 the output is going to get translated to f1 plus all multiples of k fs, this is fs, this is fs and so on. So, the H sub k of j 2 pi f for the sampler is going to be is 1 over Ts for all k. So, what this means is that, and this is 1 over Ts for all k and for all f. So, what this means is that H sub k of j 2 pi f plus fs is also equal to 1 over Ts.

And if I choose k equal to minus 1, I mean in other words, a special case of this is that when I choose the input frequency to be f plus fs and if I choose k equal to minus 1, they basically it is 1 over Ts and but we know that H 0 of j 2 pi f is also 1 over 2 s, 1 over Ts. So, what this is telling us is something we knew already, namely that whether you have an input tone at f plus fs or an input tone at f, the output is going to be exactly the same. So, there is no way of being able to discriminate between an input at f plus fs and f, in fact, there is no way of being able to discriminate between an input at f plus k fs and an input at f. So, this is simply restating this phenomenon of aliasing.

Now, so the system is, the system here as you can see is LPTV at fs, here what happens? Well, I mean, you can actually go through the harmonic transfer functions of the individual channels, like we did yesterday. And what would we observe, we will observe that the, it is only the only harmonic transfer functions which will not be 0 R. So this output can be written as sum over l of H sub 4 l, j 2 pi f 1.

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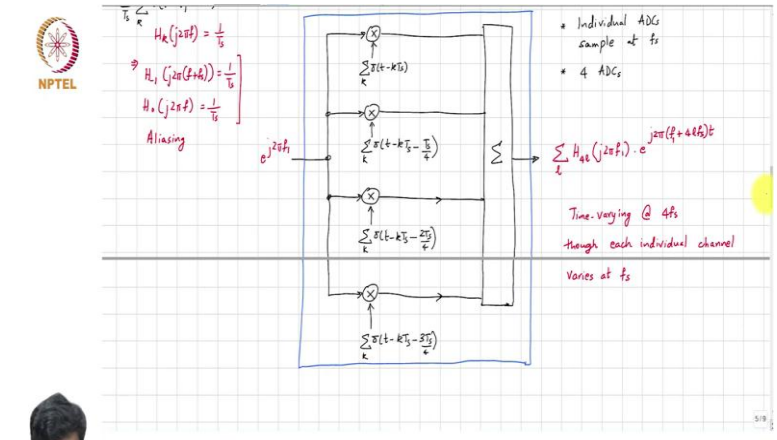

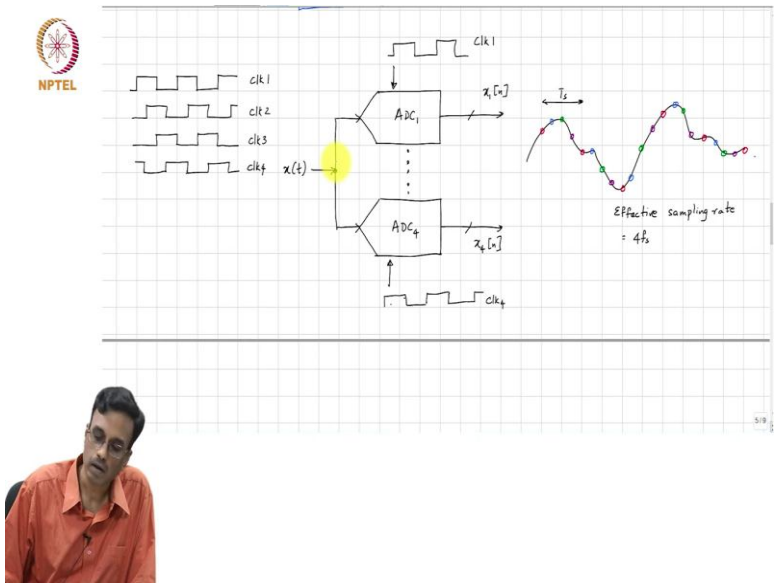

So, if that is you excite this with e to the j 2 pi f 1 times e to the j 2 pi f plus 4 l fs times t. And so, yeah, we can see, therefore see that this system is time varying at 4 fs rather than fs even though each individual channel varies at fs. And so, this is the principle, in practice of course, how this is realized is the following. So, you have 4 A to D converters and remember each A to D converter has a clock so, this is clock 1, so if you have not seen an A to D converter before, do not worry about it. This is the digital output let us x 1 of n, this is the x 4 of n.

Now, the input is let us say varying like this and this is clock 1 and this is the clock 4. Let me draw, it has to be delayed by 3 quarters of a period, this is clock 4. So, in other words, if we draw the clock waveforms let us assume that this is clock 1, this is clock 2 then this is clock 3, this is clock 4. And so ADC 1 samples here and then its next sample is here, here, here, here and here. Our ADC 2 will give these output samples.

So, ADC 3 will give, yield these output samples and ADC 4 will yield these output samples. So, the effective sampling rate is so this is remember this is Ts, the effective sampling rate is 4 fs, even though the individual ADCs are operating only at fs. Now, the next thing that I like to talk about is even though the principle is simple in practice this is a lot more complicated and the reason is the following, what will be assume, we assume that the n-path, the 4 paths or the n paths that make up the n path system are all exactly identical.

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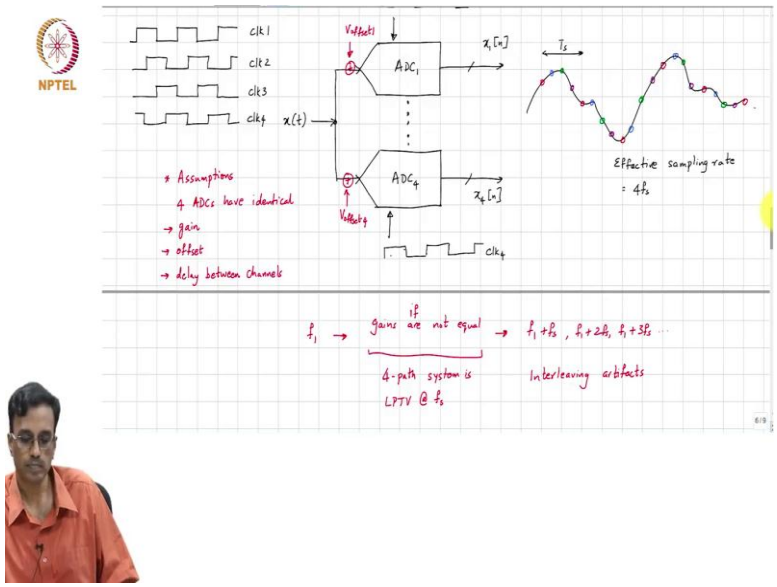

So, assumptions are 4 ADCs have identical properties like gain, offset remember that any A to D converter will have an error a DC offset. So, this is obviously an error, so the moment you have different offsets in the 4 channels then the 4 channels are no longer identical, if the, every ADC is going to have a slightly different gain and our whole n-path principle rests on the fact that the 4 paths are exactly identical. So that when you add them together the they all the corresponding harmonic transfer function is perfectly cancelled.

Now, if the gains are slightly different, the cancellation will not be perfect. And the next thing we assumed was that the delay between each one is exactly Ts by 4. And of course, in practice, you know, even though you intend to delay the clock exactly by Ts by 4, there is always going to be a small skew. So, this is often called timing skew, delay between channels. So, if you put in an input tone at f1 and if the gains of the 4 ADCs are not equal, what comment can we make about the output sequence?

Student: Cancellation (())(24:06)

Professor: The cancellation will not be perfect. So, the system will actually be LPTV at what frequency, it will be LPTV at frequency fs. So, if it is LPTV at frequency fs what could you expect to see at the output? What all tones would you expect to see at the output?

Student: (())(24:32)

Professor: Exactly. So, if the gains are not equal the 4 way, 4 path system is LPTV at fs correct. So, if you look at these, if you look at the output samples of this 4 path, this time interleaved A to D convert, this is called time interleaved A to D conversion, you will see

tones at f 1 plus fs, f 1 plus 2 fs, f 1 plus 3 fs etc. So, and I mean similarly, you will also see tones at these frequencies, if the timing skew between, if the time delay between successive channels is not exactly Ts by 4.

So, these are all practical non idealities in time interleaved ADC array and so, this is, these are all called interleaving artifacts and fair amount of work is needed to make sure that these interleaving artifacts are either sufficiently small by design or calibrated out during manufacturing or adaptively calibrated out during operation.

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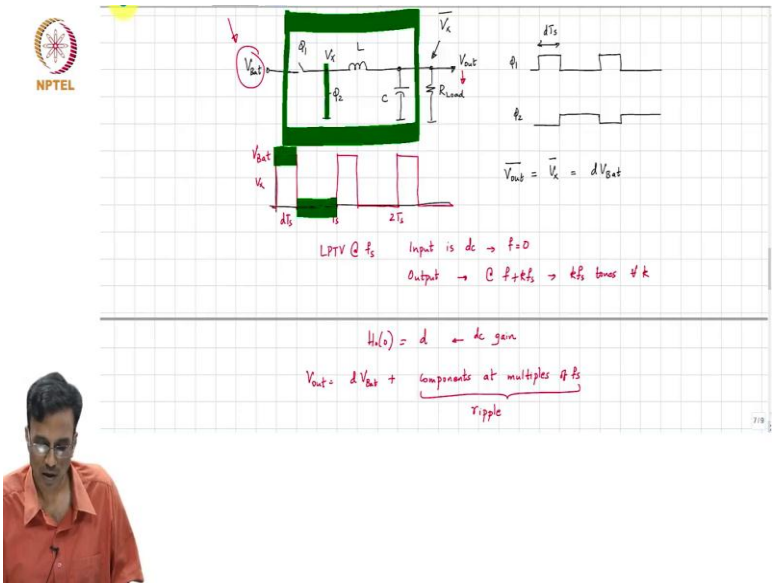

Other examples of n-path systems (involve), I mean I am not going to cover them in detail or even mentioned them in detail. So, one example is a dc-dc converter. So, here is, we want, we, let us call it V bat and I mean your cell phone, your battery voltages can be as high as 4.2 and can keep discharging and become lower. But may most of your electronics especially in the low voltage digital electronics works with a much smaller supply voltage. And therefore, there must be an efficient way of converting the high battery voltage into a low voltage. And that is done by what is called a dc-dc converter.

And here is again for those of you who have not seen this stuff before, this is the load, this is phi 1, this is phi 2, this is d times Ts, this is phi 1 and this is phi 2, phi 1 and phi 2. The switches here are at least ideally they are supposed to be lossless and are non-overlapping. So, the waveform V x at that point basically looks like, and this is V x. So, when the switch is on, I mean when the switches are closed, this is when phi 1 is high, this switch is closed and the voltage V x is basically the bat.

When phi 2 is closed, this switch is closed and the voltage goes to 0. Now, this therefore is a square wave with a duty cycle of d and the LC network here its job is to simply behave like a low pass filter. And as you can see the switches and the inductor and capacitor are at least in principle, they are all lossless.

So, the two things that one needs to observe this voltage therefore, must simply be the DC value of the waveform at x. So, this must be simply the average value at x, the average value of the output. So, in other words, the average value of the output must be the same as the average value of x, and what do you call and therefore, this must be equal to d times V bat.

So, this is a way of getting a lower voltage from the battery voltage without losing, in principle without losing any power. So, this is an efficient way of stepping down a voltage, it turns out that you can also use this to a similar kind of circuit to step up the voltage. So, this is basically what you call the dc-dc converter. Now, clearly, you can see that this is time varying system. So, how can you I mean, if you look at this through the lens of an LPTV system, what is the input frequency? What is the input, the input is DC, correct? So, what should you see at the output?

Student: DC plus fs.

Professor: Yeah, so I mean, this you can think of the dc-dc converter as an LPTV system at fs, input is DC that is f equals 0. So, the output must be at frequency f plus k fs, which was basically the tones at, for all k, and clearly H 0 of 0 is simply the duty cycle d because the input is nothing but the DC gain. So, we will see, I will continue with this in the next class.

So, this is the basic operating principle behind the dc-dc converter. Next, we will see it turns out that the dominant, I mean depending, I mean these tones at multiples of fs, so the output V out is d times V bat plus components at multiples of fs and this is what is called ripple at the causes, we will look at the nature of the output waveform tomorrow and we will see what can be done to reduce this, one way of reducing the ripple is to use N-path operation, and we will see this tomorrow.