Power Management Integrated Circuits
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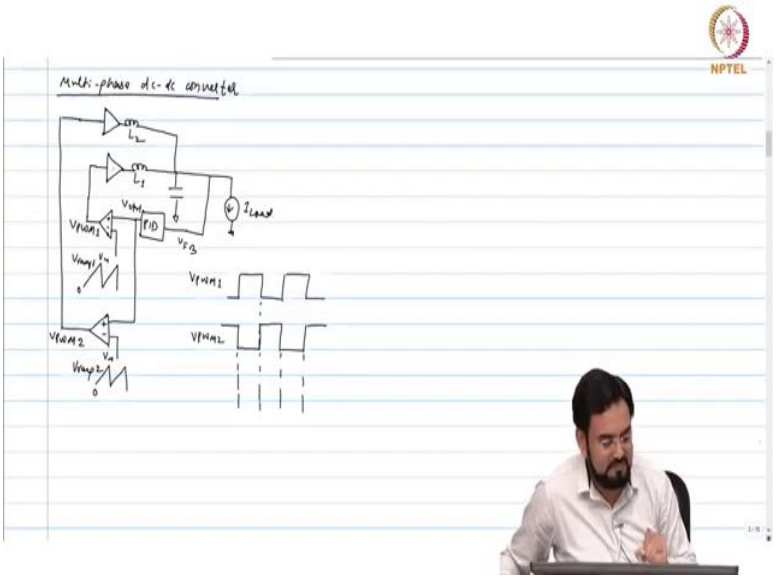
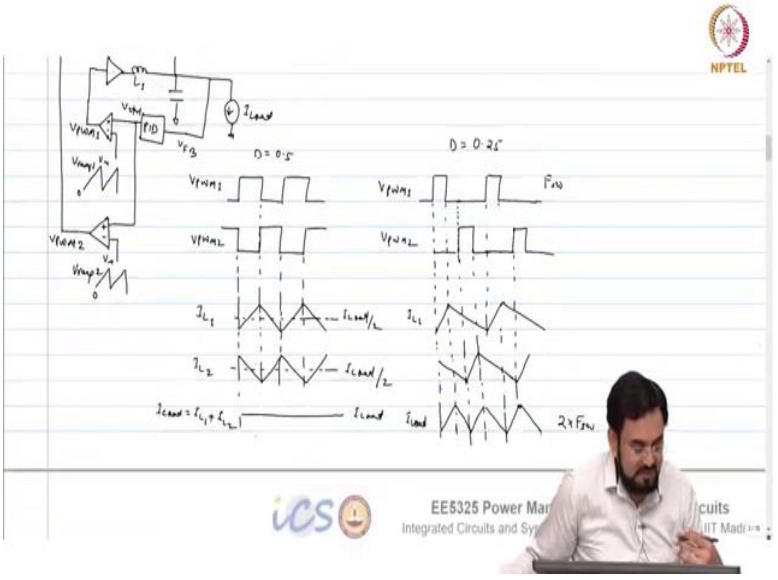
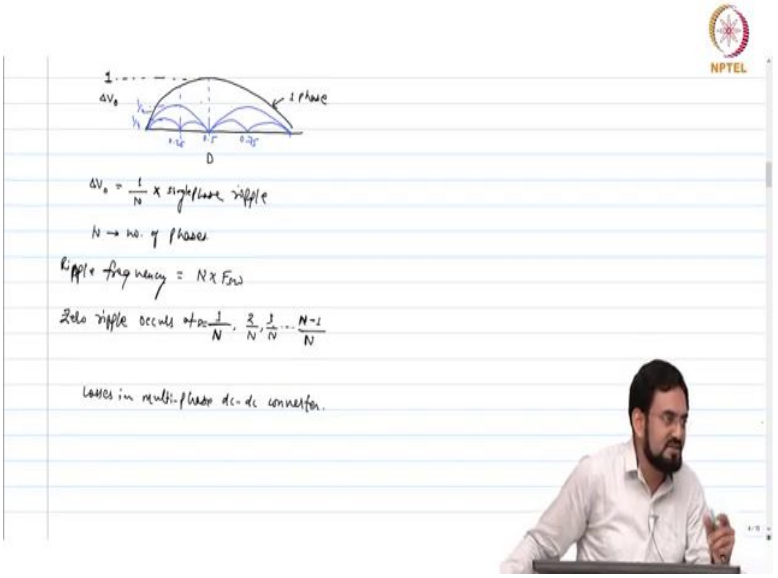
Lecture - 96
Multi-Phase DC-DC Converters



The above image shows the multiphase DC-DC converter. We have 2 PWMs and the duty cycle will be the same. Your V_{ctrl} is common and your V_{ramp} has the same amplitude.So, duty cycle should be the same but we keep them out of phase.



Current waveforms for both inductors are shown in the above image for different duty cycles. When you add the inductor current of both the inductors for 50% duty cycle, you will see no ripple. When you add the inductors currents for 25% duty cycle then the frequency of ripple will be double of the switching frequency and we know that ripple will reduce on increasing the frequency.

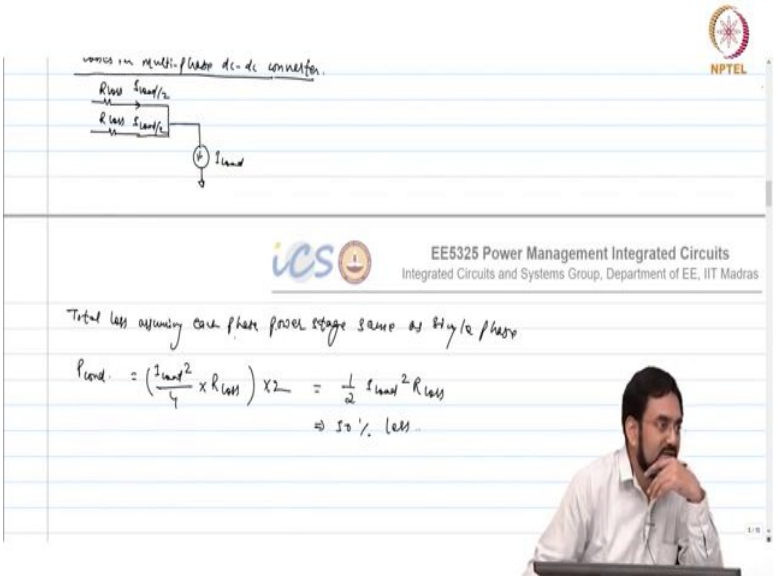


Voltage ripple vs Duty cycle plot is shown in the above image for 1 phase, 2 phase and 4 phase DC-DC converter. Maximum ripple voltage will be single phase ripple voltage divided by the number of phases. Ripple frequency will be switching frequency multiplied by number of phases(N). Zero ripple occurs at 1/N,2/N,3/N-----,(N-1)/N. Number of zero ripple points will be N-1.

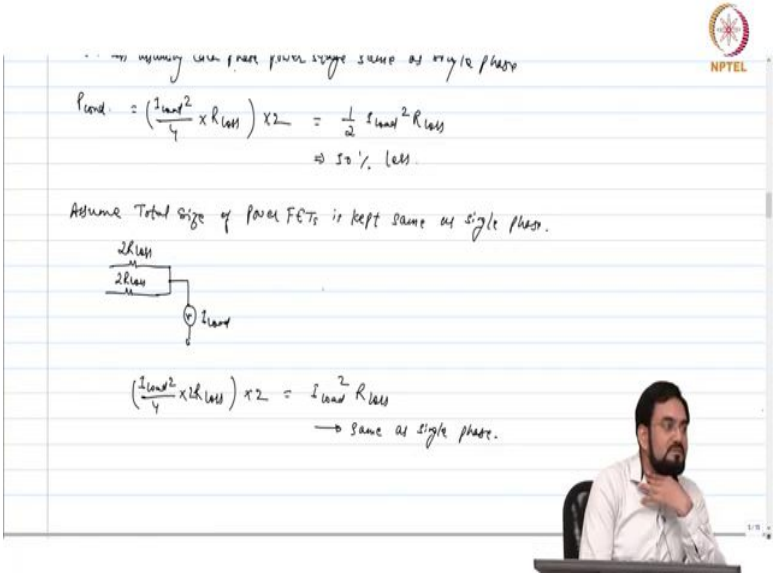
Ripple reduction is one of the advantages. But the disadvantage is that it took more components, more number of inductors, more number of power stages. Even let us say the controller is not taking too much area and your control is common, you would require extra PWM modulators only. So extra comparators will not cost you much, but power FETs are very large and the inductor is also an external component. So, it is making the cost almost double.

So, what do you do? You equally split the power FET. So, instead of sizing the same, let us say you require 100 milliohm for 1 amp. And now it will be catering only 500 milliamp, so, split into half. So, that your total area of power FET remains the same but we cannot reduce

the size of the inductor. Capacitor you can reduce because now the ripple frequency is double. You will require half of the cap for the same ripple. If it is a 4 phase converter then one-fourth cap is required. But you cannot change the inductor, the inductor is carrying the same frequency ripple, same amplitude, and the only difference is carrying lesser current. So, what can we do? We can use a higher DCR inductor that will have a smaller size. Lesser the DCR, bigger the inductor is because it requires thicker coil. So, low power inductors will be smaller in size compared to high power inductors. You can get maybe 20-30 percent reduction by using lower power inductors here.



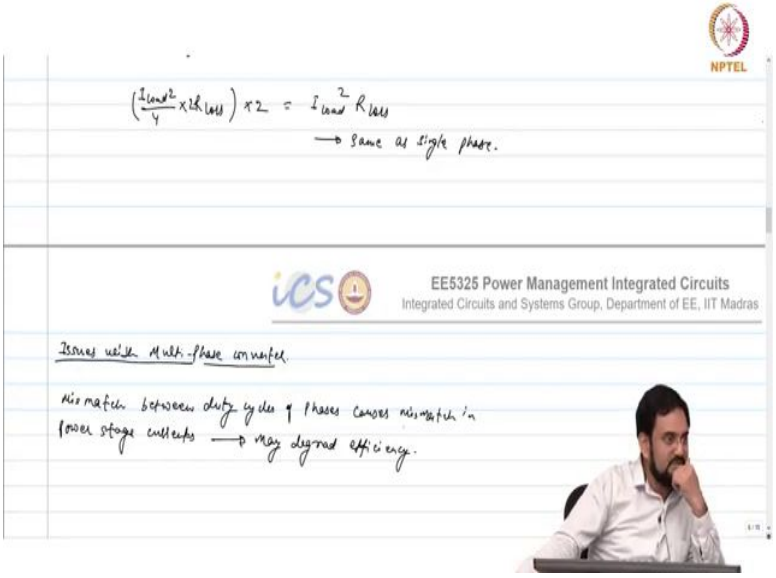
Now, let us see the losses in multi-phase DC-DC converters. Calculation for conduction loss due to inductor is shown in the above image. If you use the same size of inductors, then in multi-phase your conduction losses will be lesser because each phase is carrying only half the current.



If the inductor DCR is double compared to the single phase inductor then losses will be the same as the single phase DC-DC converter. Calculations are shown in the above image. You may not benefit in terms of losses, but still the benefit is in the ripple. You can achieve the same ripple with the smaller cap.

But now let us say if the same thing I want to do for the boost, you know current is boosted there. See your inductor current is I_{load} over 1 minus D. Let us say I am operating at 50 percent duty cycle. So, 1 amp current load current, inductor will be seeing 2 amp current. Now, split in the 2, each will be seeing only 1 amp current. So, there you may get more benefit compared to buck in terms of losses and losses will cause heat and sometimes you may require a heat sink. So, the size of the heat sinks depends upon how much loss is in your converter.

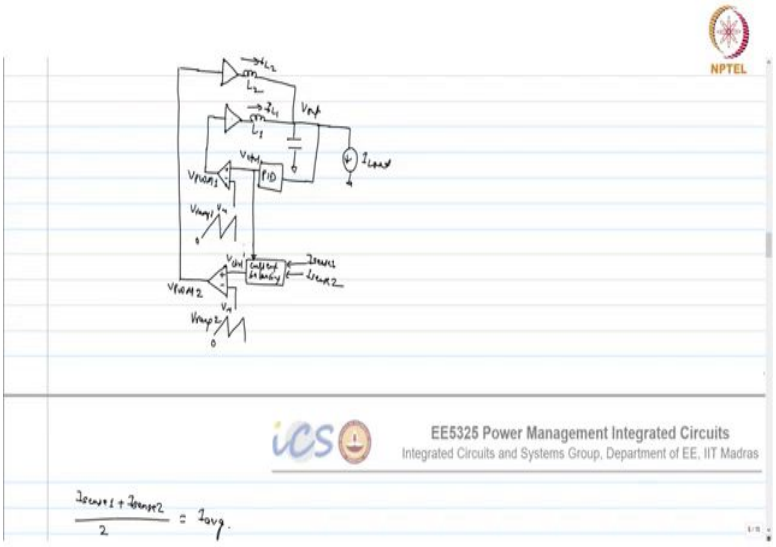
So, you can reduce the size of your heat sink in a multi phase compared to a single phase converter. And same thing you can do if you are using the same inductor and same power stage but at the extra cost.



There is one very common issue with multi-phase converters. So, all the assumptions are that both the inductors are carrying the same current but who will decide they are carrying the same current or not? Capacitor will not decide, capacitor is carrying only ripple current. If both the inductors have the same R_{DCR} then they will carry the same current. But we cannot ensure that. Let us say if the DCR of one inductor is higher compared to another inductor then current will not equally split and the inductor with lesser DCR will have more current flowing through it. If the current is not equally split then it is not a problem because If R_{loss} is more thenI want to reduce the current and difference in DCR values will automatically do that. So, it is actually an advantage. If there is R_{DCR} mismatch then the current in the inductor which has a lesser R_{DCR} will be more.

The problem is if there is a duty cycle mismatch then there will be current mismatch in both the inductors. Even if there is a duty cycle mismatch, your loop will force in such a way that your average duty cycle will look the same and there will be no problem in regulation, the problem will be current balancing that is caused by mismatch in duty cycles. Let us say this duty cycle mismatch in such a way that instead of carrying 500 milliamps each, one goes 600 milliamps and the other goes to 400 milliamps. The one which is carrying 600 milliamps will see a higher loss compared to the other inductor. On an average it is quite possible that average loss may be higher compared to if currents are equally split. So, that is why we require current balancing here.

We are using a single control voltage. So, it will not cause mismatch. Ramp, comparator offset or delays in the comparator will cause the mismatch. In ramp, we are charging a capacitor with the current and those two currents may have a mismatch.



So, that is why we require a current balancing. in the current balancing what do you do actually? You take this control voltage.So, instead of connecting like common each one will have so, let us say if this is I_L2, I_L1 instead of either writing (Refer Time: 28:53) equal to how much?., I_sense2 ok, same thing you do on the other side. So, what you take the V_ctrls and you take the sense current from both actually, so I_sense2. So, what is the current required at each phase?

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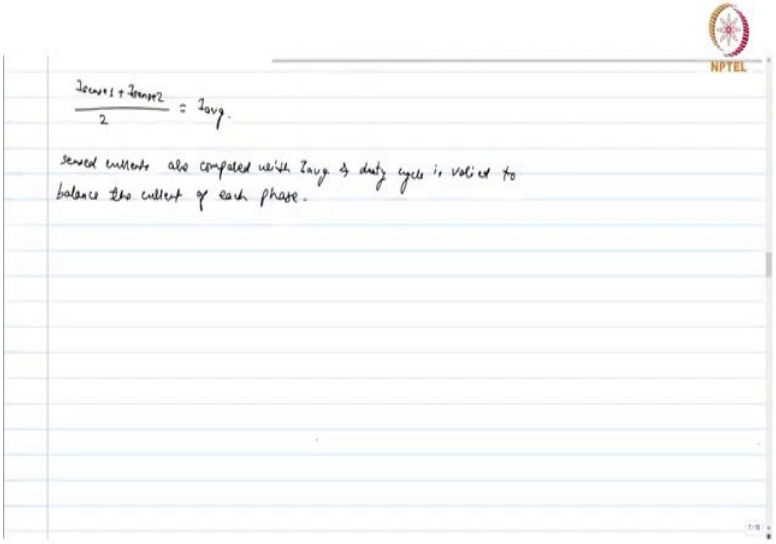

I_sense1 plus I_sense2 divided by 2 equal to I_avg. So, you compare each current with I_avg and see it's higher or lower, and then based on that you decide whether duty cycle needs to be increased or decreased. So, same thing is required, we do not have a space here, but same thing is required on the other side also. Because you do not know which one needs to be increased or decreased, ok.

So, basically you have to do in one side you have to increase, other side you have to. So, let us say 600, 400 milliamp instead of 500 600 milliamp has to be 500 milliamp. So, if you just reduce it by 100 milliamp and the other side has to be increase by 100 milliamp. So, you compare with the average whatever they require and we are already. So, this requires your current sensing and we know how to do the current sense sensing. So, it requires extra hardware, extra complexity of those they are in multi-phase. So, this is the main problem which with the multi-phase.

Student: They are like if there is a balance due to R_dcr then also it will get values due to their.

Yeah, it will do. So, in this case it will always it does not care about why it is. So, but when it balances with the different R_dcr then the impact in efficiency is very small, compared to if this mismatches is due to the duty cycle. And you can do that calculation because that mismatch I mean that R_dcr is already very small. So, that mismatch will hardly impact 1 or

2 percent mismatch or even 10 percent mismatch LC efficiency impact would not be that much.

But if we create a 1 percent difference in the duty cycle, that efficiency impact will be huge achieved. So, that is why you do not care about, even if it reduces your efficiency due mismatch in inductor little bit, you do not care because that impact is not as high as mismatching duty cycle. But if you have a weight where you determine whether this mismatch is due to R_dcr or due to duty cycle.

Then and that that is also quite possible you can both measure both the duty cycle at the switch node. So, this you can always measure the duty cycle at these 2 P_sw 1 here and here. Ultimately you are a interested in the N duty cycle.

Student: Instead of having this sense current like if we lock duty cycle only.

Yes, you can do that, most of time we do like. If you can measure their duty cycle in a very high resolution manner, I mean 0.1 percent or so you can do that. But, in the time based we do not get that problem actually because you tap the phases and they are already all phases of matched. I mean the delays will cause a mismatch. So, I mean let us say I have a 5 delay cells in the ring, I have five delay cell. So, it is a 5 phase I can tell 5 phase from there and but ensuring the each delay cell is exactly same or matched it's very difficult. So, the phase-to-phase mismatch maybe there, that may cause difference in the duty cycle multi-phase.

So, in that case what we do? Instead of running the VCO let us say I want 10 mega Hertz, I will run my VCO at 50 mega Hertz and then, divide it by 5. So, if again I will get a 10 megaHertz, but since they are divided, overclock and then divide, so, all the phases will be matched perfectly matched. So, you will not have any mismatch problem and that is what we did here actually if you see.

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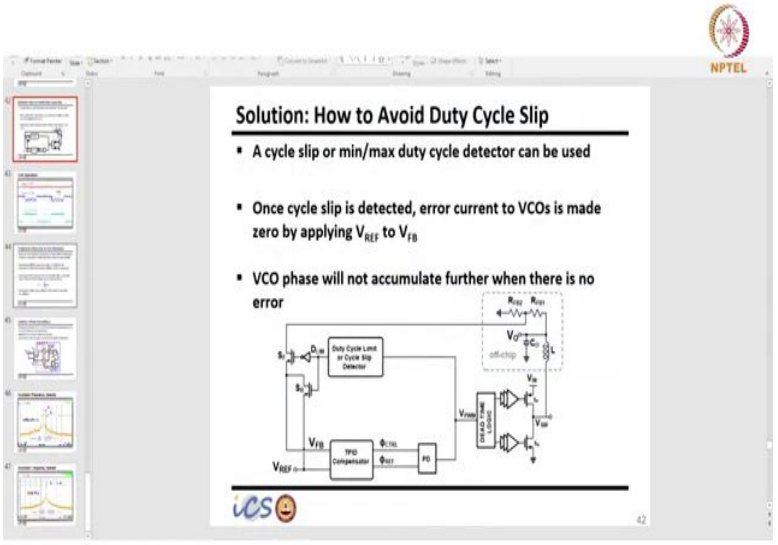

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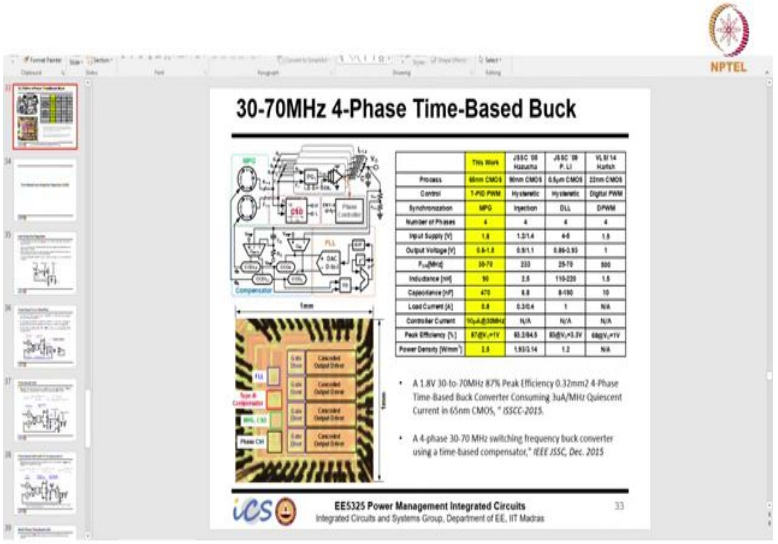

So, this current. So, here actually its 1 to 4 phase we are tapping and this whole VCO is running at if its 70 mega Hertz, then 70 into 4, 280 mega Hertz actually, that is what it is running at this VCO.

And then here it is nothing but, you can think of multi-phase generator is nothing but divided by dividing this clock by 4 and separating out all the 4 phases. So, single phase goes here at

4x and then separated out in 4 phases rather than tapping the 4 phases directly from the VCO, because that may have mismatch.

So, here you get a very good phase matching; do not, but the VCO are is running at 4x so it will have some extra current obviously. But if you compare this at extra current by running the VCO at 4x and what complexity and the current you required to generate for the current balancing and all those, that is much simpler here.

Because current sense itself is not simple. So, each sensed compared with I_avg and duty cycles that is valid to each phase. So, you can subtract there depending upon if you know how much it is, which is required or it may have its own integrator also. Because you are comparing something, it will generate a error that error can be accumulated and that code digitally you can change the correct the duty cycle or you can implement in analog way and change, add or subtract the voltage from V_ctrl which is going to the comparator. So, now this will be V_ctrl', I will call it semi control ok.