Power Management Integrated Circuits
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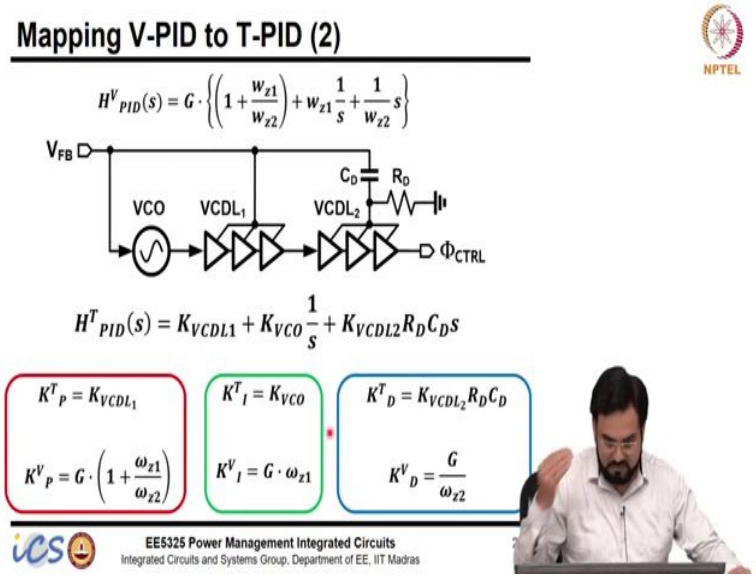
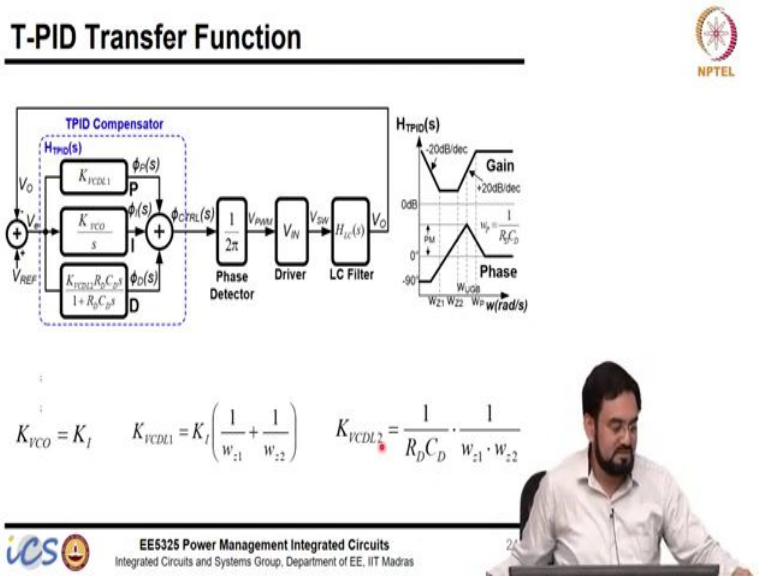
Lecture – 95
Time-Based Controller for Buck Converter and for LDO, Issues with Time-Based Control

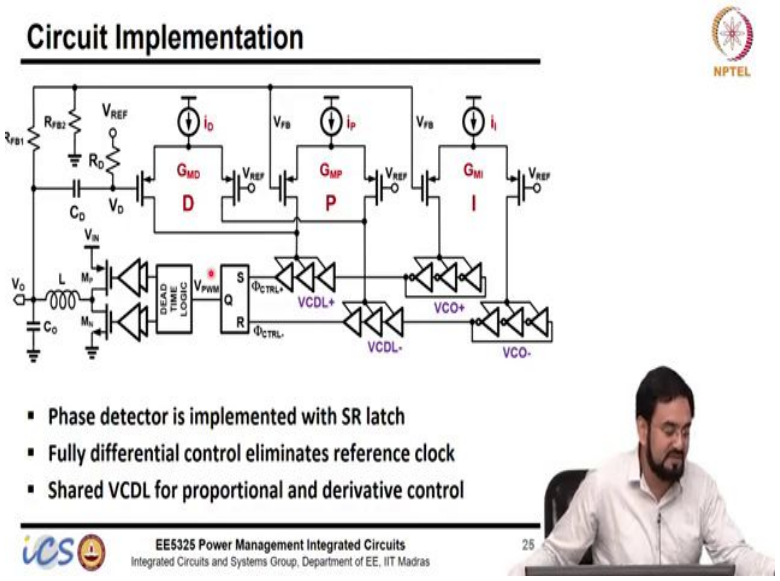


So, we were talking about this time based DC-DC converter, how you build the control loop in the time domain using VCOs and VCDLs. So, we can build all the integral proportional and derivative and cascade them and we know delays are added or phases are added by cascading. So, simply we will get the output voltage which will have all the three components: proportional, integral, and derivative. We know what are the proportional, integral and derivative in voltage domain. We can simply map them and find K_{VCDL}, K_{VCO}, K_{VCDL1}, K_{VCDL2}, R_D and C_D.



So, if you want to model we can model like K_{VCDL1} is in our proportional gain and then K_{VCO} by s will give you an integral component and this is your derivative component which have one pole, we have to make sure this pole should be outside your UGB so that it will behave like a differentiator. So, 1 over 2pi is the gain of the phase detector; here phase detector is a modulator. So, just like in the voltage domain we had a gain of $1/V_m$, here we have a gain of 1/2 pi. Then V_{in} is your power stage and then H_{LC}.

If you do the loop gain analysis you will see a similar behavior here you will have two zeros and 4 poles. One pole is outside UGB, one is at origin which is integrator and two complex poles from H_{LC}. There are two phase detectors. You can build the phase detector simply using XOR gate. In that case, the range only will saturate at pi but if you are using a flip flop pfd that will give you 2 pi phase difference.

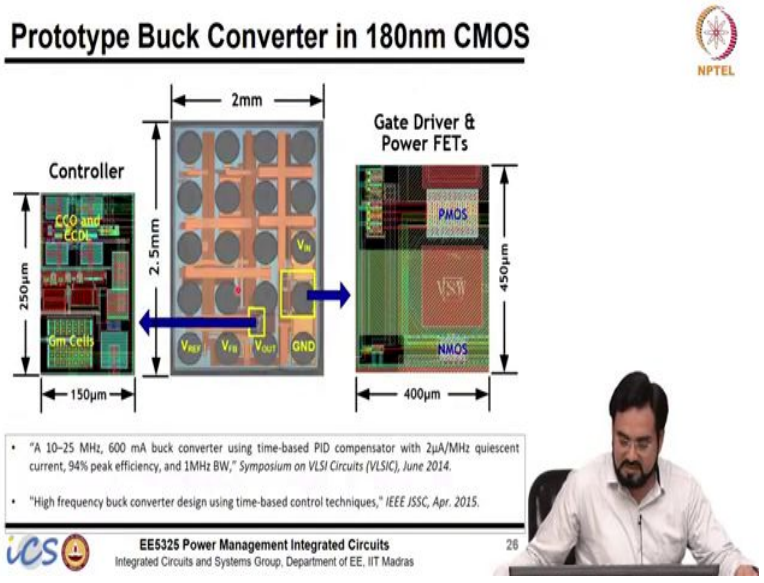


It depends how you implement it. In this case, we have implemented simply using SR flip flop. You have two clocks with a phase difference. If I set at one edge of the clock and reset at the other edge of the clock then your total range you will get 2 pi. So, the way we implemented it instead of using a VCO which we call voltage control we are using current control. We are controlling the delays with the current and my feedback and reference are in voltage, so I need to convert that into current and we can simply use transconductors. So, what we are using here at the input you can see. This is actually your derivative component because it is you having a first order high pass filter compared with V_{ref}. So, this will be biased at V_{ref} so that we get only high pass components here. It will not pass any DC component.

This is proportional. So, we simply compare V_{ref} with feedback voltage and then this is your integrator which is VCO. So, what we have done actually, instead of using two separate VCDLs we used one VCDL. We know that we are converting voltage to current and we are having a separate voltage to current converter for the two. So, we can sum up and use only one VCDL. So, one VCO for integrator, one VCDL for proportional and derivative. P and D are already added in the current. So, we do not need another VCDL here. You could have separated it out and this output should have gone to a different VCDL, but we are already getting a P plus D component. So, why do we need to add one more VCDL.

You can see it as a fully differential and the advantage of fully differential is that relative loop delay is almost 0 here. Let us say, instead of using this I could have used only VCO output here directly not the VDCL. Now, what would happen, if this VCDL delay changes this VCO delay will not change. Across PVT, free running frequency may have some delay and if those delays are matched then relative delay is 0 but if they are not matched then let us say with the temperature or process this delay is changing and this remains fixed then this will add to a loop delay and it may hamper your transient response.

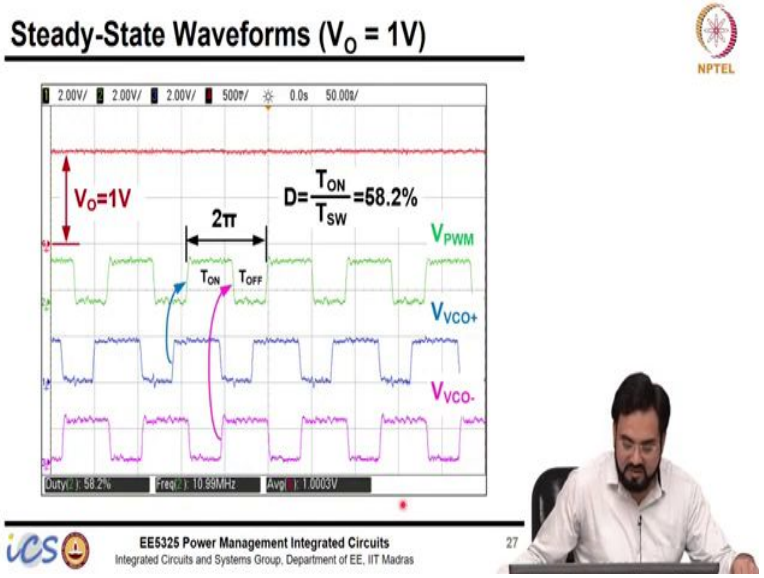
But in this case, let us say with the PVT this delay is changing and this is also changing, so both are changing in the same direction. So, relative delay is zero and there is no loop delay. The only delay you will get in the power stage due to finite rise and fall times. So, the controller has no delay just like in the voltage mode we have a reset time delay your comparator had delay all those delays are 0 here. And that was the main reason we can push it at much higher frequency. At one edge we set and on the other edge we reset. So, this SR flip flop will simply behave like a phase detector.



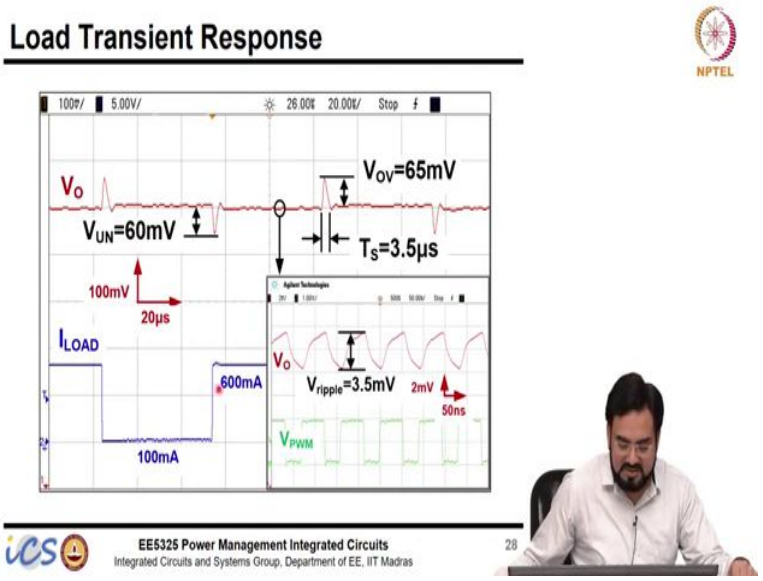
This was the chip we implemented. So, this is your power FET, power FETs usually are bigger and this is the controller. The advantage here is that the controller is very small because it is hardly using any large passive components. We have some capacitors here. One was required for your derivative component, the first order high pass filter. And then we have some decoupling capacitors. But they are very small, like an order of a few picofarads, you

can say compared to what you would have required let us say 50 to 60 picofarad capacitors in the case of voltage mode. If you are limited in area and you can reduce the size of your controller then it will give you more room to have bigger power FETs and you can have smaller $r_{ds\text{-}on}$.

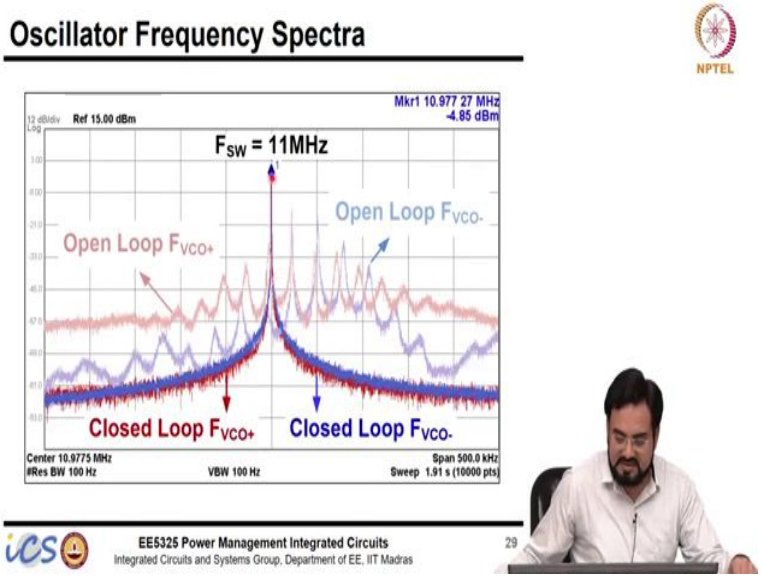
We implemented for 10 to 25 MHz switching frequency and maximum current was 600 milliamps and this was consuming 2 micro amp per megahertz. Quiescent current is very low here. So, at 11 megahertz, it was consuming 22 micro amps. That is why we are coding it as 2 microamp per megahertz.



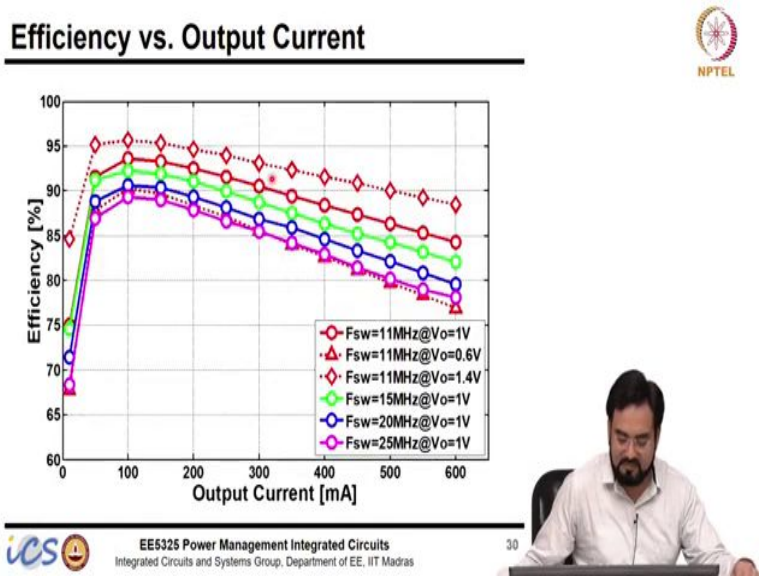
These are the outputs of VCO plus and VCO minus and this is your final PWM which gives you the phase difference between them. So, duty cycle will be nothing but the phase difference between the two. You can say that this edge is not synchronized with this because we are taking VCO output not from the VCDL, VCDL will also have some delay. So, we took the VCO output that is why you are seeing that difference. But ultimately, the difference between this edge and this edge is nothing but the duty cycle.



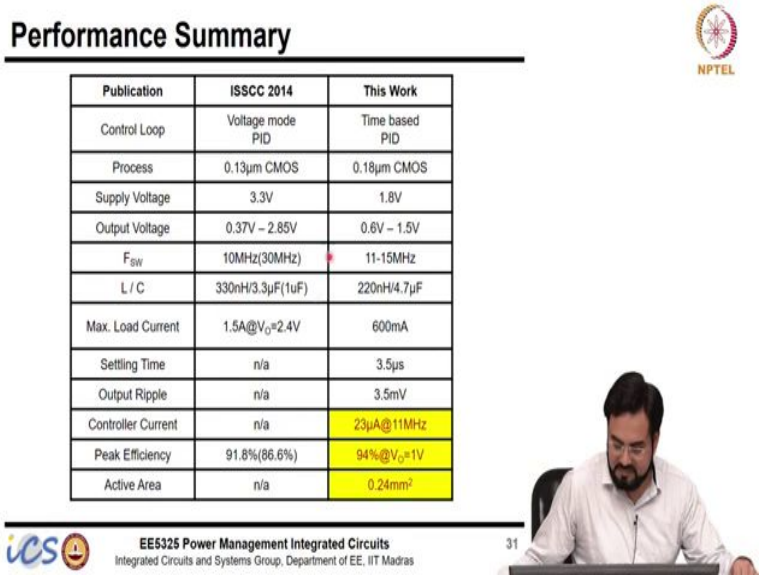
This is a transient response. So, 100 milliamps to 600 milliamps which is 500 milliamps load step and undershoot overshoot is roughly 60 millivolt here. This is under the lock condition.



So, if we operate in the open loop then the loop will never force to lock the two VCOs. So, both VCOs are like on their own and they can go anywhere. That is why you can see frequencies moving all over the places, but the moment we close the loop both VCOs are locked at 11 megahertz here.

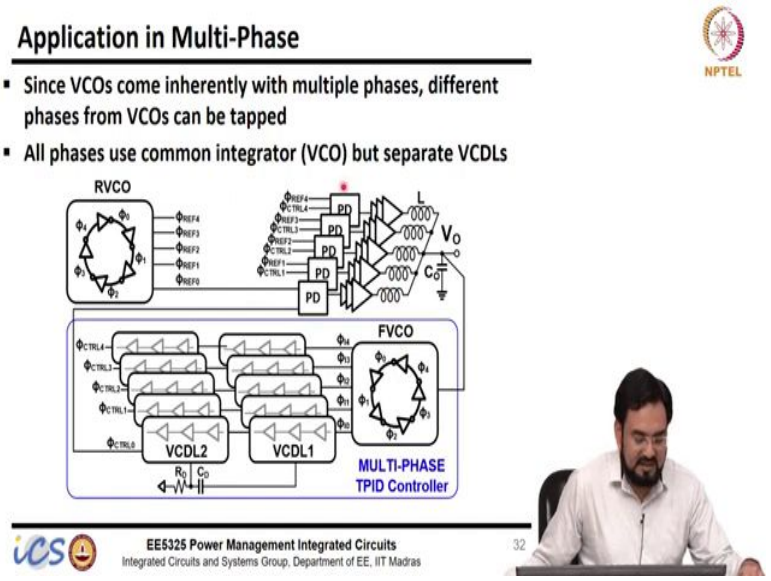


This is the efficiency at different frequency and output voltages. So, the maximum we achieve at this one is 11 megahertz and 1.4 volt and the switching losses are higher at higher frequency. So, 25 megahertz will give you less efficiency because CV square f losses are higher.



Publication	ISSCC 2014	This Work
Control Loop	Voltage mode PID	Time based PID
Process	0.13μm CMOS	0.18μm CMOS
Supply Voltage	3.3V	1.8V
Output Voltage	0.37V – 2.85V	0.6V – 1.5V
F_{SW}	10MHz(30MHz)	11-15MHz
L / C	330nH/3.3μF(1uF)	220nH/4.7μF
Max. Load Current	1.5A@V_O=2.4V	600mA
Settling Time	n/a	3.5μs
Output Ripple	n/a	3.5mV
Controller Current	n/a	23μA@11MHz
Peak Efficiency	91.8%(86.6%)	94%@V_O=1V
Active Area	n/a	0.24mm²

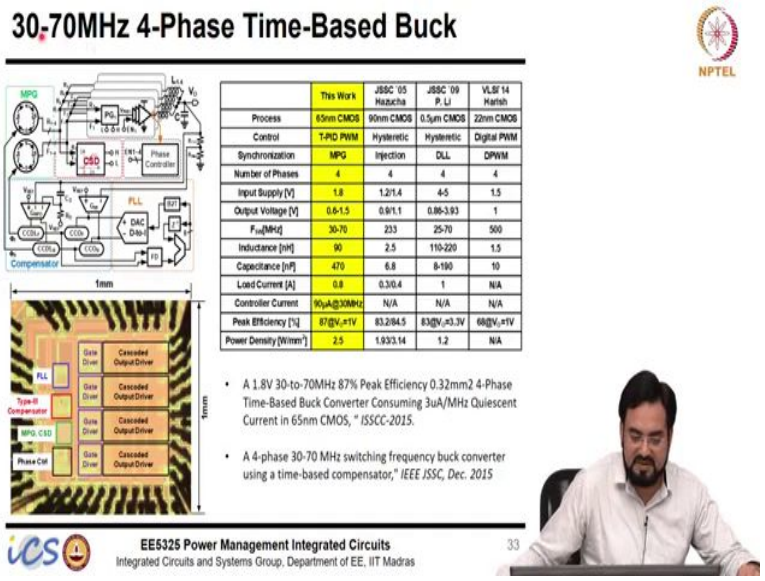
This work we implemented in the 0.18u process and 220 nano inductor and 4.7 microfarad capacitor because we are running at beyond 10 megahertz, so we do not need the inductors in the order of microhenry here.



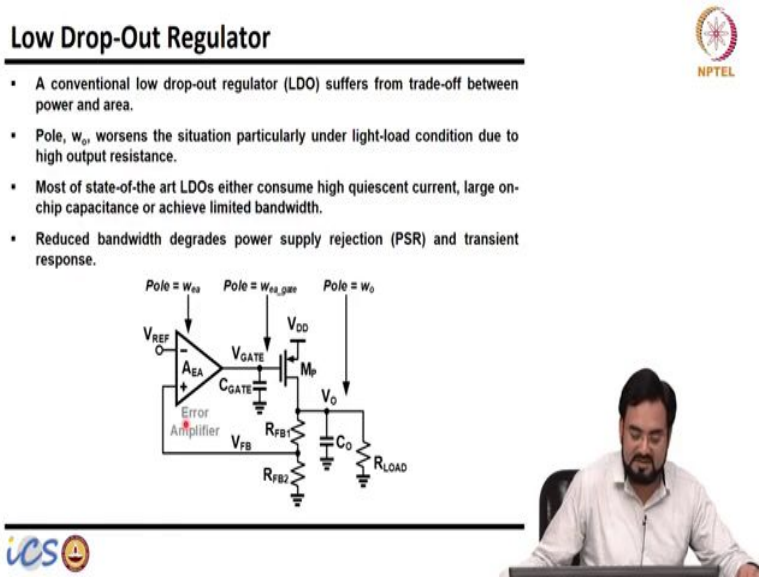
Another advantage is that we can go for a multiphase converter. I will talk about the basic concept of multiphase later. The benefit in using multi phase here because VCOs are ring oscillators and inherently we have multiple phases here. So, all you need to do is just tap all the phases and pass to different power stages which will have their own inductor and the capacitor will be common.

So, that is how the multi phase is implemented, it is like parallel converters and the load current will be shared among all. So, let us say if I have a 1 amp current and there are 5 phases here. So, 200 milliamp will flow in each phase. So, that is how you reduce the power stage current. Your I square R losses will be less compared to the single phase.

So, when we implement very high current let us say 10 amp or so then the only way is to use multi phase. In a single phase, we cannot handle it because it's very difficult. So, that is the advantage. But if you have to implement the multi phase in standard voltage domain. These phases are equally spaced. So, we need multiple ramps generated at different phases, here we are getting all the phases for free. All you need is just a copy of the same VCDL1 VCDL2 and replicate them and just feed them different PFDs and that will drive your power stage.



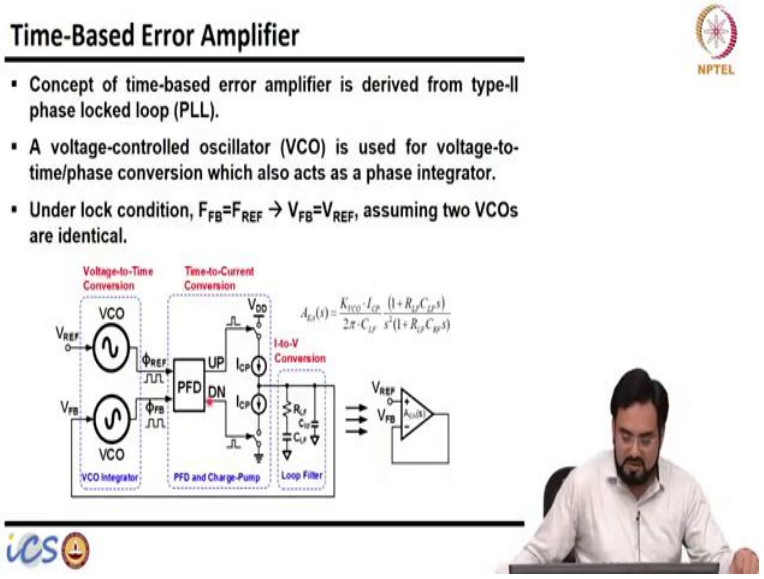
In this one, we went up to 70 megahertz 4 phase time based buck and peak efficiency 87 percent. Since we are using more phases so the power consumption at 30 megahertz is 90 micro amps. So, per phase here it's roughly 3 micro amp which is almost similar to what we have in the previous we are at 2 micro amp it is 3. This is your power stage and look at the controller size, it is pretty small. Then recently we started doing LDOs using time based.



We already talked about what are the issues with the LDOs and how you compensate for it. We know there are three poles in the whole system. One is with your error amplifier and most of the time we make sure that the error amplifier pole is pushed outside your UGB.

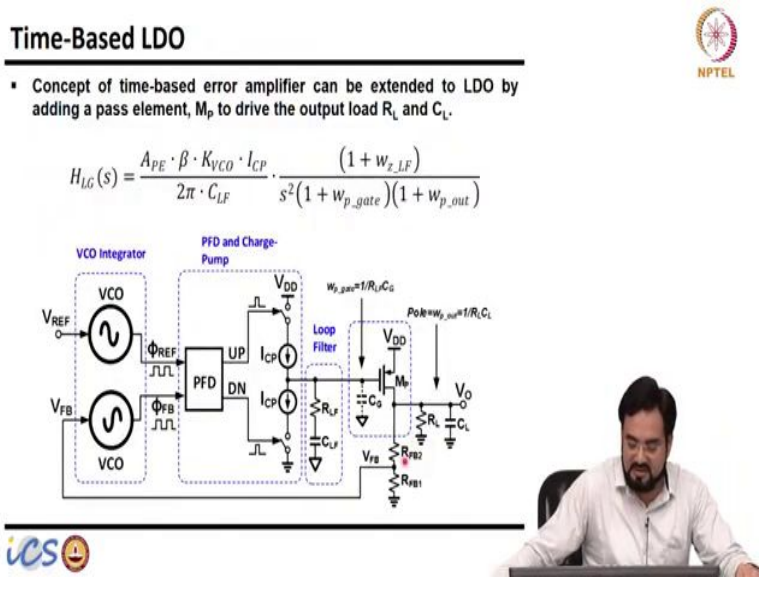
Then we are left with two poles one is your gate of your power FET and then output pole. So, usually we use a dominant pole compensation or miller compensation and make sure that the pole at V_{gate} is inside your UGB and this output pole is outside your UGB. So, which means we are limited in bandwidth and PSRR will also degrade and if I want to increase the bandwidth, then we have to move both the poles at higher frequency. So, let us say I have designed something for this LDO for 60 degrees phase margin and I want to increase the bandwidth, I have to make sure both poles move proportionally. So, that your phase margin is maintained.

So, which means I cannot put a large cap at the output. If I put a large cap here then the pole will start moving inside then you have to limit the bandwidth or make the output pole dominant, output pole dominant means you have to make sure that the impedance at this node is very small. So, you may require to add some source follower or some buffer. So, the R_{out} at this is much smaller so that this is pushed outside and this will start dominating in that case and we know at higher load this impedance will go low then again it will start moving outside. So, we have to make sure the separation is again maintained. So, the capacitor requirement will be much higher at maximum load. So, these are the issues like there is a tradeoff between bandwidth and your PSRR and your transient response and obviously the cost. If I want to improve the PSRR I have to increase the bandwidth and increase the bandwidth means higher power consumption.



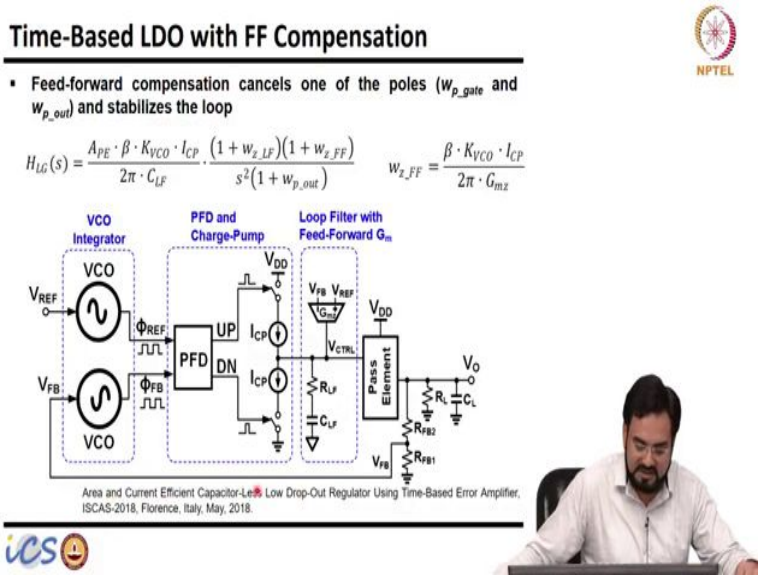
Again the same concept, use two VCOs which will act as a reference and feedback. And now I am using PFD in the previous case I was locking only frequency, now I am locking phase also. So, I need a charge pump because you need to remember here in the previous case I needed an output as a PWM but in a linear regulator there is no PWM. So, I need to convert that time back into voltage and that is why we are using a charge pump. So, phase detector will give you the signal more looking like a PWM and this will be converted back into a voltage by modulating this current and then you have a loop filter that will filter out all the high frequency signals and give you the DC.

So, now, we have two integrators here one is VCO and another integrator is in the charge pump because current is dumped into a capacitor. So, I need one zero here. So, two poles are there and we need to cancel one. So, this series R will add a zero and it will cancel and this capacitor will cause another pole which will be at 1 over R_{LF} C_{RF}. So, this parallel combination of these two we have to make sure that is pushed outside your UGB otherwise it will become unstable. So, now, this is behaving like a unity gain feedback amplifier and if you look at a LDO it is nothing but a non inverting amplifier but with a high current drive that is the only difference. So, this cannot drive high current. So, we need to add power FET. We can use it as an error amplifier and connect the pmos at the output.



It will now start behaving like a LDO and now we have two additional poles. So, we have two integrators and then one pole is at the gate just like a traditional voltage based LDO and

another is at the output. So, we have to make sure that one of them is cancelled out. So, we have added only one zero, now we need to cancel one more pole here.



So, I need one more zero. So, what we did actually we added a feed forward zero here through the gm. So, now, you have two zeros, the zero we due to this gm will be beta K_vco into I_cp over 2pi G_mz. And if you do a derivation you will find that actually what that or you can refer to the paper we have given there the details about how these zero comes all you need to just apply kcl here you will get yeah one is outside your.

So, in this case you required three zeros. So, we have to make sure one of these poles outside your UGB just like a traditional voltage mode LDO we cannot have both output and gate this pole at gate inside UGB. So, that requirement remains there you have to make sure that one of these are outside UGB. So, only one pole is left. So, we need to cancel only one whether it could be output pole or pole at K.

So, the advantage here is this error amplifier is behaving like a like an ideal error amplifier I mean your gain in the in the standard voltage mode gain is limited by gm r_out here there is no gm r_out as such gain is not limited by that I mean you can say that your impedances limited by this node ok, but it does not matter that impedance your gain is. So, even no matter what do you have if there is any error that will be integrated into this VCO and it will correct.

So, ideally it has a infinite gain actually. So, you can build a like 200 300 dB kind of a gain which is not possible with the voltage mode. So, your accuracy will be only limited by the offset not by the gain here.

And second advantage is now I can build a very high bandwidth amplifier without burning too much current here and you can operate at lower voltage also. Because I mean if you want to build a very high gain error amplifier then you need to cascode obviously, or gain boosting and you cannot operate at very high voltage here all those requirements go away actually.

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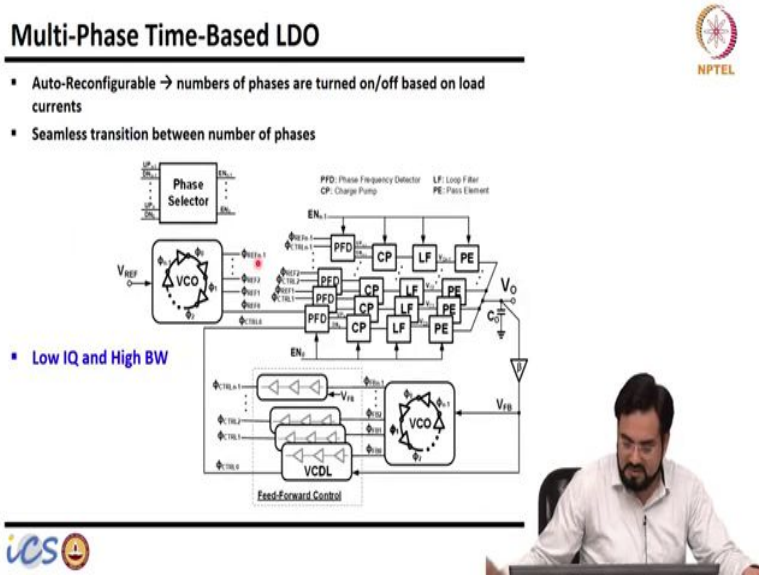

So, the same concept which we use like multi phase in switching DC-DC converter, you can use a multi phase in LDO also.

So, the advantage here is I have all the power FET's parallel connected in parallel you can think about there are multiple power FETs each one has its own this PFD and charge pump, but we are using common VCO, because we cannot have multiple integrator in one loop, and they will start fighting with each other. So, we can have only one integrator, but we can have multiple PFDs and charge pump. So, each will have its own control and. So, now, the advantage here is depending upon the load current you can decide how many phases needs to be turned on.

So, let us say I want to cater 10 milliamp 10 milliamp is. So, you will size your power FET according to 10 milliamp. Now let us say I have 10 phases. So, I will size. So, each phase is carrying 1 milliamp. So, I have to size one power FET for 1 milliamp only. And now they are connected in parallel. So, whenever my current requirement goes above 1 milliamp only then I will turn on second phase when it goes more than 2 milliamp I will turn on third phase. So, that is how I will keep on turning on and off depending upon the load vary. So, the advantage here is now the capacitor seen at the gate in light by each phase is very small. So, you can increase the bandwidth without increasing too much current and another advantage is look at the light load. So, if you oversize your power FET, then you go very low current that will saturate that will go in sub threshold and saturate it may saturate also.

But in this case your power FET is very small. So, at very light load only smaller component is on and even you can make it even smaller whatever you want to you can keep one phase let us say to handle only 100 micro amp.

So, that and that will be only that will be on and the gate cap will be very low you can still have a very high bandwidth without needing very high current basically. So, that is the advantage here if you scale number of phases or power FET sizes with a load current it is similar concept what we used in DC DC converters to reduce CV square f losses if you remember segmented FET.

So, the same concept is applied here actually. So, it will give you very low I_Q with high bandwidth. So, this multi phase also we published last year this was 2018 that was 2019 the multi phase one. So, I mean everything looks good, but there are; obviously, since it is a new technique. So, it will come with some issues and we need to find a solution for that.

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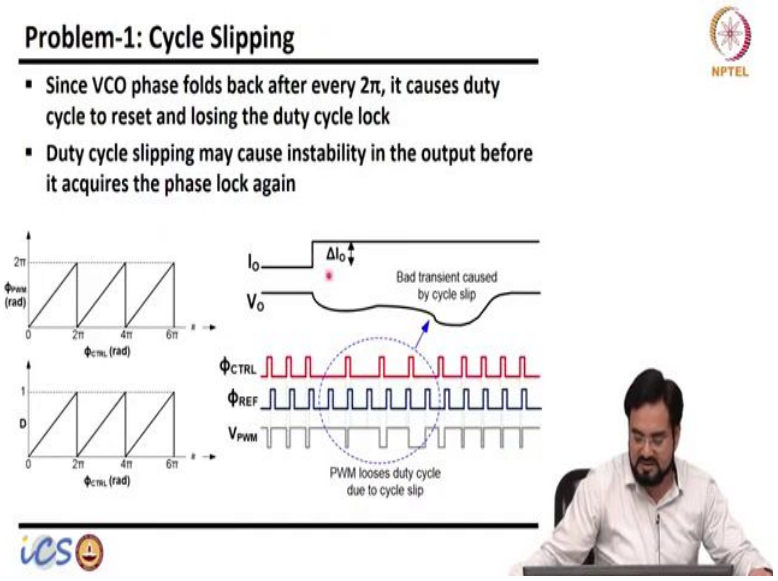

So, one we talked about your cycle slips. So, the moment your phase crosses because phase will always fold back to 2pi. So, from 2pi to again 4pi. So, it will behave like a. The range is only 0 to 2pi. So, to 2pi will become 0. So, duty cycle will reset to 0. So, let us say you are operating at a very high duty cycle which is shown here.

Let us say 90 percent or so transient comes and so your phase will change and it will accumulate and it will try to go to 100 percent which is 2 pi the moment it crosses 100 percent it will cross and make it 0 and you will see output will dip.

So, which means I mean this is more like a failure actually system failure because it may go out of regulation and reset your whole system which is unacceptable.

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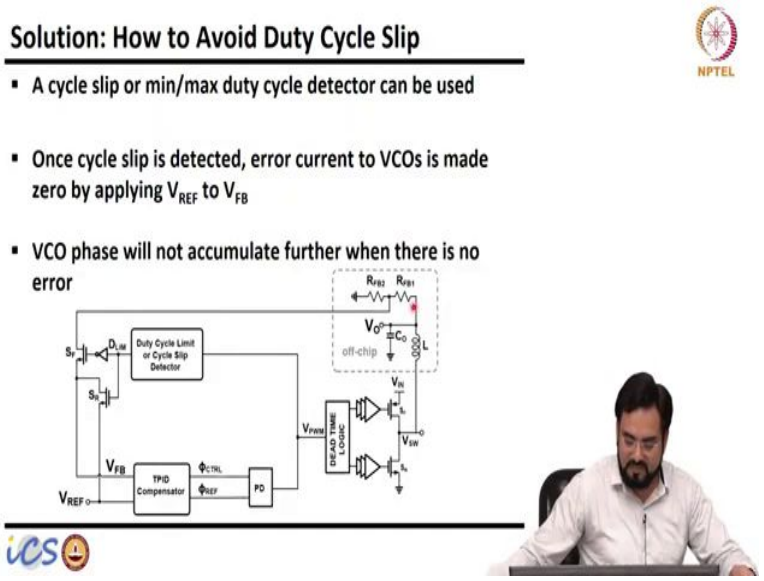

So, we have to prevent this. So, how we prevent actually prevent it. So, what do you have we have actually I mean we know the phase will only accumulate when there is error and if I know I can define a maximum and minimum duty cycle and whenever I detect the maximum or minimum duty cycle I make the error voltage 0. So, that is what I am doing here.

So, duty cycle limit or cycle slip detector; cycle slip detector is more like you can say which detects 2pi phase. So, either you can look at the duty cycle or look at the phase difference in both the cases you can take the decision. So, whenever it goes 2 pi you make the error voltage 0.

So, what we are doing here whenever this duty cycle limit or cycle slip is detected. So, we know one end is connected to V_ref other is connected to V_fb. So, we removed the V_fb and connect V_ref through this FET and make the error voltage 0.

So, when the error voltage 0 the phase will not accumulate and it will not try to go towards 2 pi and when it comes back to your steady state then you again it will automatically. Basically your dealing will go 0 in that case it will only reach when it tries to cross the maximum duty cycle. So, it will come back and then output will get settled. So, you will not see this kind of behavior.

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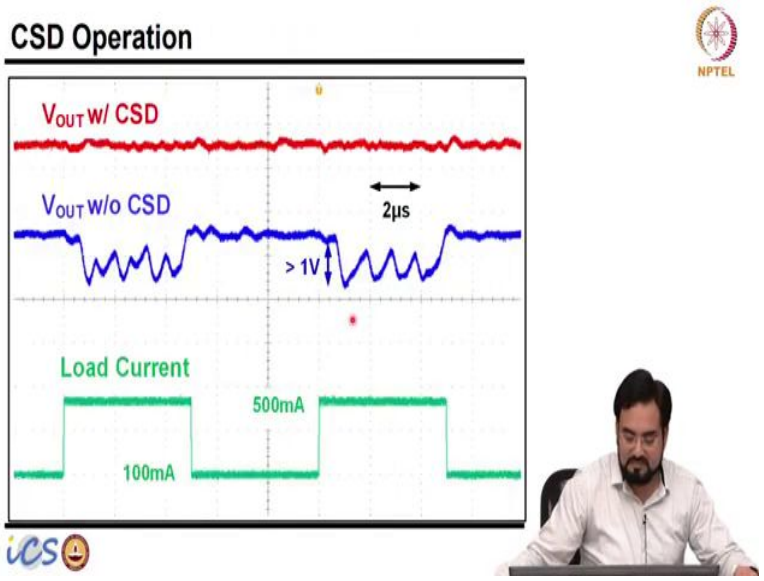

And you can see this is with cycle slip detector when we apply the load current the duty cycle is changing and going to 2pi and my voltage dips like this undershoot you can see its more than 1 volt actually.

So, if you are operating at 1.2 volt it will go to like 200 millivolt or so and the moment I have a cycle slip detector then it remains constant rate.

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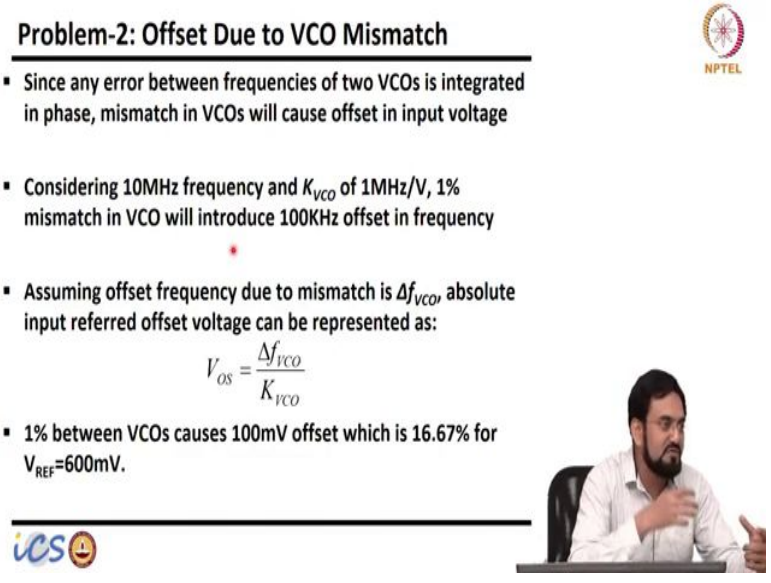

Another problem is offset due to VCO mismatch I mean. So, far we are considering that these VCOs are matched. So, if they are matched then when V_fb equal to V_ref then the frequency will also be same, but if let is say there is a mismatch then what would happen even if the V_fb same as V_ref the frequency will be different and when the frequency is different the phase will get accumulated.

So, what will happen ultimately the loop is trying to lock the frequency it does not care about what the input voltage is if they are not matched then what will happen the frequency will match at a different feedback different feedback voltage then V_ref and that is what will cause the input referred offset.

So, if we want to calculate we know the K_vco; K_vco means how much delta frequency per volt. So, let us say this 1 megahertz per volt and the free running frequency is 10 megahertz means when in a steady state. When V_fb equal to V_ref then both the VCOs will have the same current and depending upon at what frequency at what bias current you have in that gm which we have a like V to I converter. So, half of the current will flow in both.

So, that will define your free running frequency. So, let us say 10 megahertz free running frequency I am taking the same case what we had in the 10 to 20 megahertz buck the first buck which we had. So, and the requirement for there was 10 megahertz free running and the K_vco we required was 1 megahertz per volt.

Now let us say 1 percent mismatch in the VCO. So, 100 kilohertz offset in the frequency correct. So, 1 percent mismatch means 1 percent of 10 megahertz is how much?

Student: 1 megahertz.

1 megahertz.

Student: 0.21 megahertz.

Yes. So, 100 kilohertz and in terms of K_vco how much is this.

100 kilohertz with respect to 1 megahertz per volt how much is this?

10 percent.

Student: 10 percent.

So, 10 percent and if you translate back into the voltage it will looking like a 10 percent offset. So, the 1 percent mismatch will be a 10 percent offset, but now my V_ref is 0.6 volt not 1 volt. So, the 0.6 volt again will be scaled 1 percent will be scaled to 16.67 percent. So, the 100 millivolt I mean so 1 megahertz per volt means 100 kilohertz per 100 millivolt correct.

So, 100 kilohertz mismatch will cause 100 millivolt offset in the voltage input voltage and my V_ref is 0.6 volt. So, 100 millivolt of 0.6 volt is how much 16.67 percent. So, this is the offset you will get actually and if you have a V_ref 1.2 volt then it will go half it will become roughly 8.4 percent or so. So, it is still very large actually I mean we know bandgap can give a maximum 1.2 volt and if I am operating at 1 volt around 1.2 volt I am forced to use the lower V_ref I cannot use 1.2 volt and get a 1 volt output in the regulator that is impossible.

So, that is why we most of the time we use lower V_ref and lower V_ref basically will translate into more offset because we have a gain here beta factor. So, how do we fix this which means we need to cancel this offset just like we do in the standard voltage mode?

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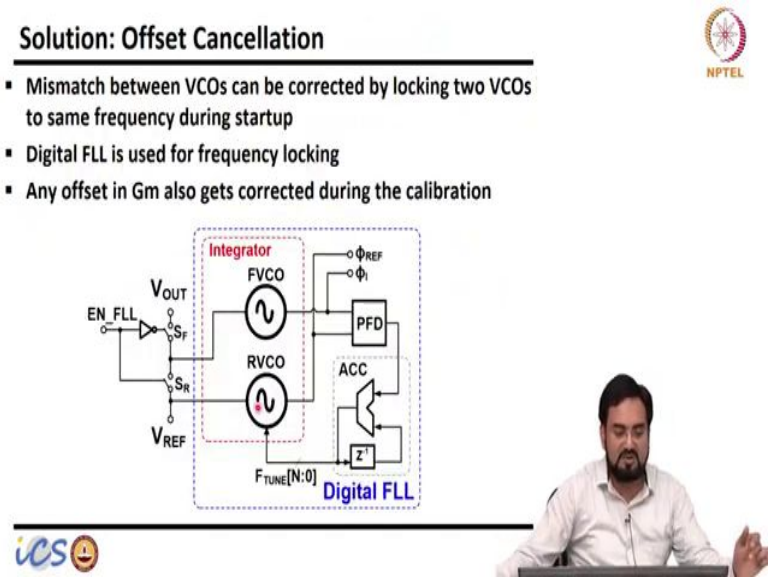

So, what we do actually during a startup again if I connect the both the VCOs input to V_ref and see if there is any frequency difference in the output or not if there is a frequency

difference; that means, there is a mismatch because both voltages are connected to V_ref. So, if they are matched both should operate at same frequency.

But if there is a frequency mismatch they will not operate at the same frequency. So, this PFD will detect the frequency and I have an accumulator that will accumulate the frequency error and control one of the VCOs.

So, if let us say this guy is higher you can reduce the this frequency or increase the other frequency whatever you want to do. So, so that is how you correct the offset. So, the another advantage is I am only showing the VCO here, but if you let us say you have this kind of implementation this one this guy.

So, everything will be in the loop. So, any offset due to this diff pair will also get cancelled out. So, the offset due to mismatch in VCOs offset due to mismatch between these diff pairs everything will be taken care in that one single FLL and after that you connect your feedback voltage back and close the loop and it will run in the normal operation it is like a static offset cancellation which we were doing in the error amplifier.

You remember we were introducing the offset in one direction by canceling the offsets. So, you have positive offset we were introducing negative offset and what we were doing? We were tying the.

No we were tying the input we were making the error 0 and monitoring the output whether it is a 1 or 0 and then keep applying when transition happens the same thing is here, but everything in the time domain that is it.

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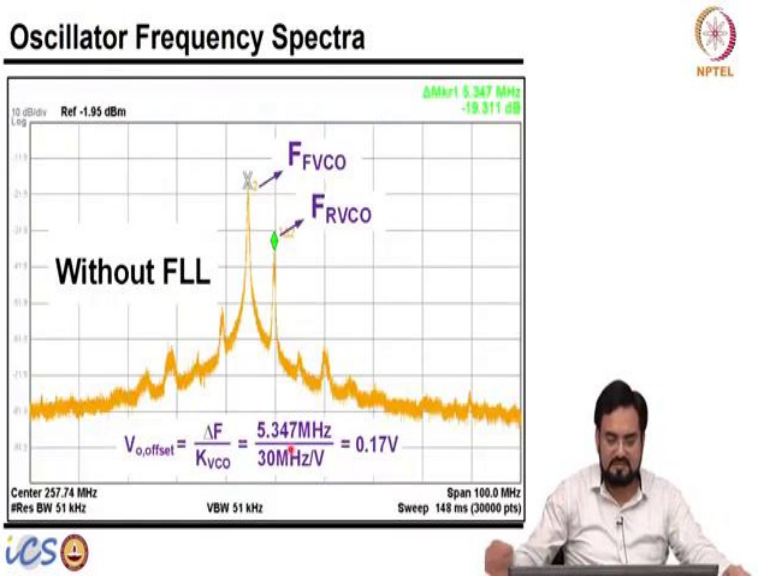

So, this is with offset and we have seen like 0.17 volt offset at 30 megahertz due to mismatch we were seeing 5 point which is like I mean much higher than 1 percent 5 megahertz out of 30.

So, it is the huge offset I mean huge mismatch you are seeing.

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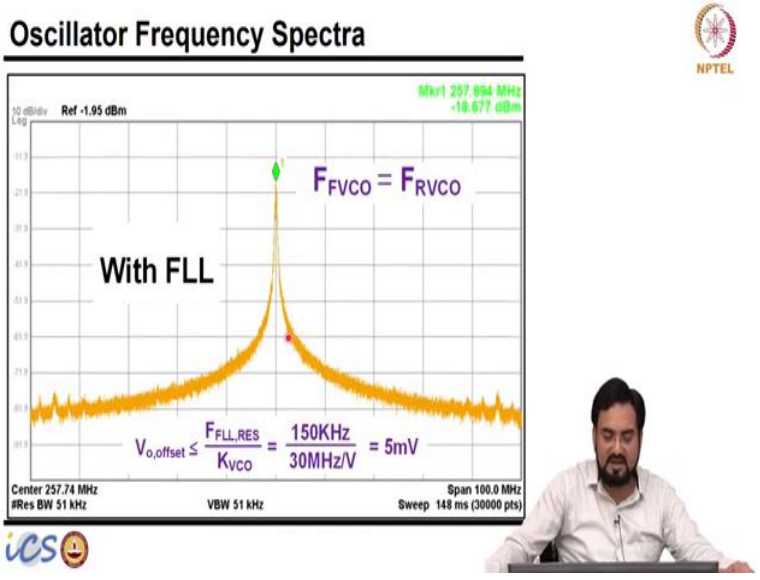

Now, we turn on the FLL and correct the offset and. So, 170 millivolt now reduced to 5 milli volt. So and how much offset maximum accuracy you can achieve it will depend on the resolution of your FLL. So, more number of bits I have in this accumulator I can tune with a finer resolution and I can reduce is further if I let us say my requirement is less than 1 milli volt then you simply increase the number of bits here in the accumulator and you can get that.