Power Management Integrated Circuits

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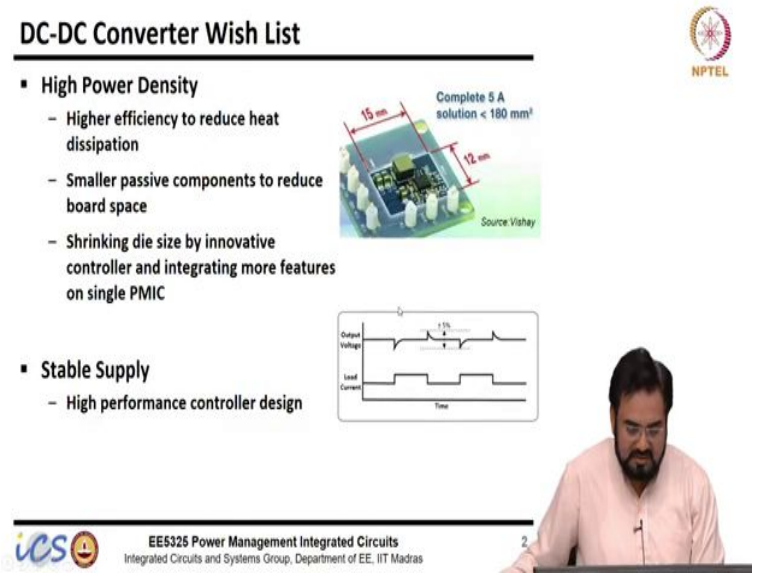
Lecture - 94
Limitations of Analog and Digital Controllers, Time-Based Controller for Buck Converter

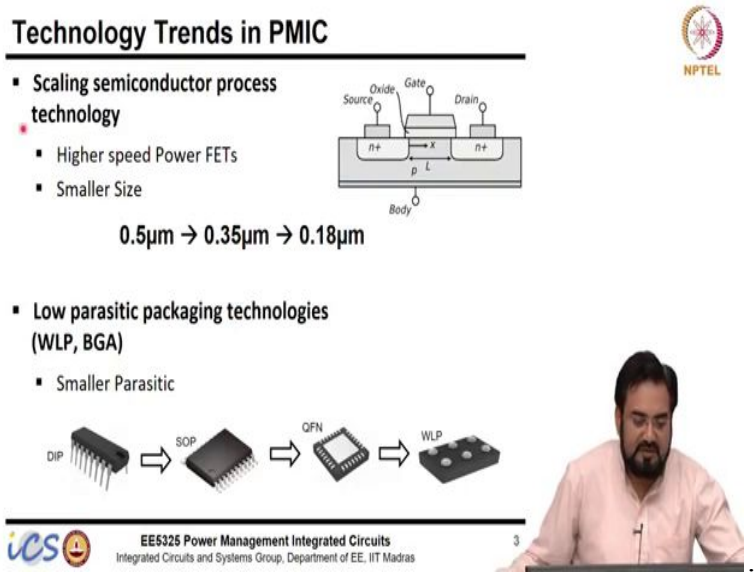


We will now move to Time Based Voltage Regulators. So, for any regulators, if we know that we need a high power density which means higher efficiency to reduce heat dissipation. Whenever you are looking for high power density then you have to achieve very high efficiency because when efficiency is poor then it is very difficult to achieve higher power density. And sometimes, it may even require heat sinks which will actually increase the size of your module. So, smaller passive components to reduce board space because I do not want my inductor to be big and this is your chip converter chip and you can see that most of the areas taken by your L and C.

So, shrinking die size by innovative controllers and integrating more features on a single PMIC means, let us say I do not want my controller to occupy more area than compared to your power FET, I want my power FET to dominate area because I am looking for lower $r_{ds\text{-}on}$.

But if the controller becomes two times of power FETs. So, that is very impractical actually. We always try to minimize the area of the controller. So, your chip size is only limited by the power FET. And by reducing the size of the controller if let us say I want to achieve 2 millimeters by 2 millimeters die size and which means if I reduce the size of the controller the extra space I can use for power FET itself and I can put some more FETs to reduce $r_{ds\text{-}on}$ further.

Stable supply means high performance controller design and we know the transient response and your output accuracy depends on how good your controller is.



So, if you look at technology trends in PMIC. We know that the semiconductor process has been scaling almost every year. And if you look 20 years back we were at 0.5 micron then maybe after 5 years or so you got 0.35 and then 0.18. It has been here for more than a decade and we still use this 0.18 because of all the features which were available here like high voltage devices. These days when you look for 0.18 high voltage process, you get 0.35 and 0.5 devices also. So, 0.35 will be running at 3.3 volts, 0.5 will be running at 5 volts and 0.18 will be running at 1.8. So, you get a different variety of devices in the same process. So that you can do all your logic in a smaller channel length and all your high voltage in the higher channel length. On the same substrate, you can have multiple devices. And if you have a BCD process you can even have 40 volt and 60 volts devices.

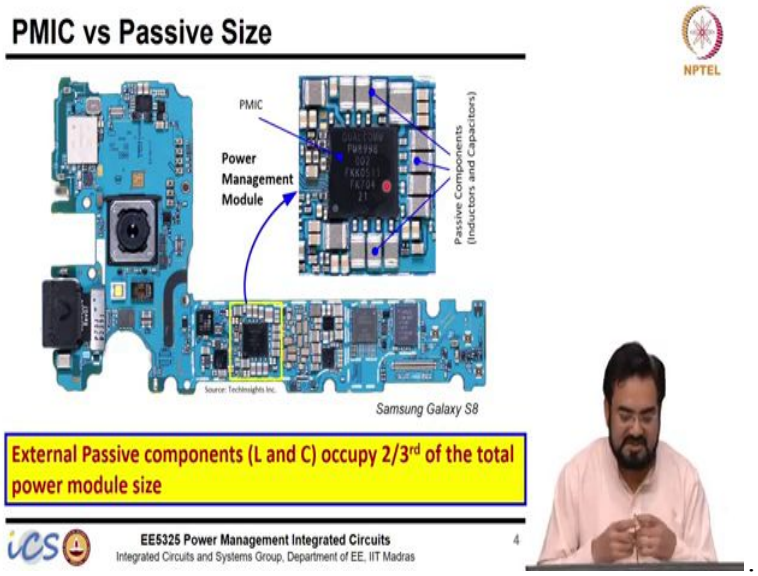
Low parasitic packaging technologies. In the old days, what you use on your breadboard was a DIP package, then we had SOP and then QFN. So, as you move in this package on the right hand side you will see the parasitics will reduce because the package parasitics are mostly driven by how the lead frame is done and how the pins are. So, bigger the package means more parasitic and your die size is much smaller. So, you have to bond and use a longer bond wire to connect your pads to the pin.

WLP is nothing but wafer level package. So, these balls actually will sit directly on the die pad. So, your die size will be the same as the package. If let us say I remove the package then your x and y dimension of that die will be the same as your package that is why we call it wafer level package.

So, this package can be done at a wafer level and then you can slice it actually, but these packages cannot be done at wafer level, you have to first slice your die and then send it for packaging and most of the time this is maybe 4 to 5 times bigger than your die.

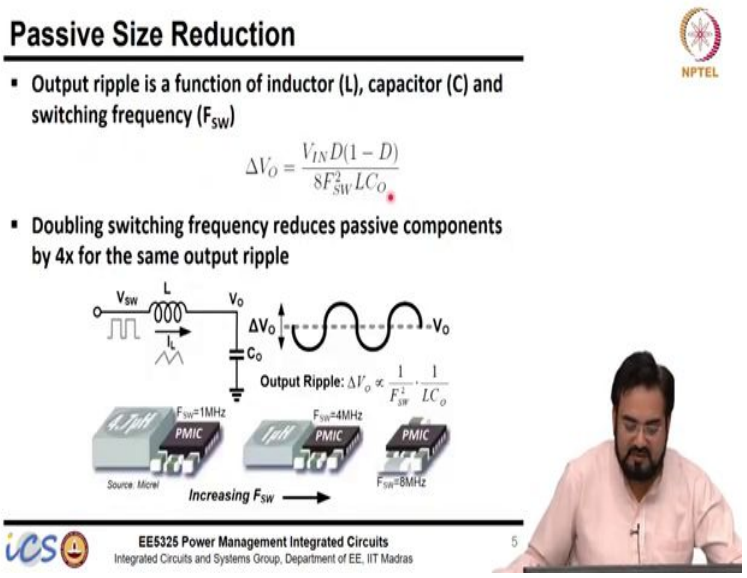
So, among these three the QFN is the best and if I have a WLP option then nothing is better than that because your parasitics will reduce. You have these power FETs and these power FETs are connected to the ground and Vdd. I do not want to add any inductor in the series because these are carrying very high switching current and the current is rising from 0 to few amps within no time. So, your Ldi/dt noise will increase if you have any series inductor there and that will kill everything.

So, you cannot have more than a few hundreds of picohenry inductor, but if you have any bond wire you can easily get a 1 or 2 nanohenry inductor and that will kill everything, especially if you are doing very high current converters. So, from a parasitic point of view, this is the best and also from a size point of view because your package is the same as die size. So, these packages are available and most of the PMIC which go in the cell phone and other devices you will see they mostly use WLP packages.



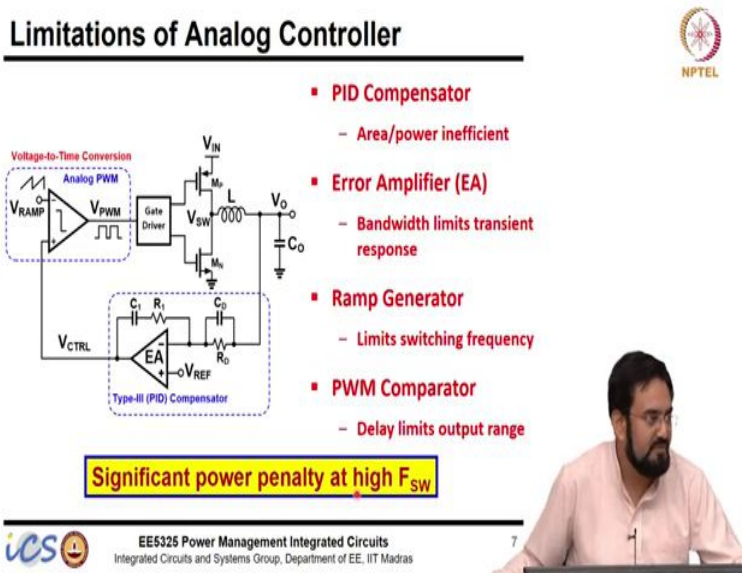
This is your Galaxy S8 and this is your PMIC. This is Qualcomm PMIC PM8998 and at the bottom, if you flip upside down you will see exactly these balls and this is a much bigger PMIC. Because it has integrated 5 to 6 switching converters and it has more than 25 to 30 LDOs inside. You have a lot of power supplies inside and other than that you have a lot of housekeeping stuff like ADCs for measurement. It has more than 200 pins. So, now, if you see this PMIC surrounded by these passive components and these are nothing but your inductors and capacitors. So, these bigger size components you see are mostly inductors and the smaller sizes are capacitors. Almost two-thirds of the total area is taken by your passive components which means the chip is not limiting your module size, but it is passive components which are limiting your module size and the chip size is very small because we are using the WLP package.

Our target should be to reduce these passive components and not to reduce the die size further because we will not get any benefit. Even if I make chip size 0, still almost 65 to 70 percent will be occupied by the passive components. It will not help much in that case.



So, for the same ripple, we know this is the formula. So, if I want to achieve the same ripple and increase the frequency let us say double the frequency, I can reduce the size of the inductor by four times or I can reduce the inductor by half and the capacitor also by half but most of the time capacitors are much smaller compared to inductors. So, we always try to reduce the inductor size actually. You can see if you are running at 1 megahertz your 4.7 microhenry inductor will look like this, I mean much bigger than combining the capacitor and your chip size.

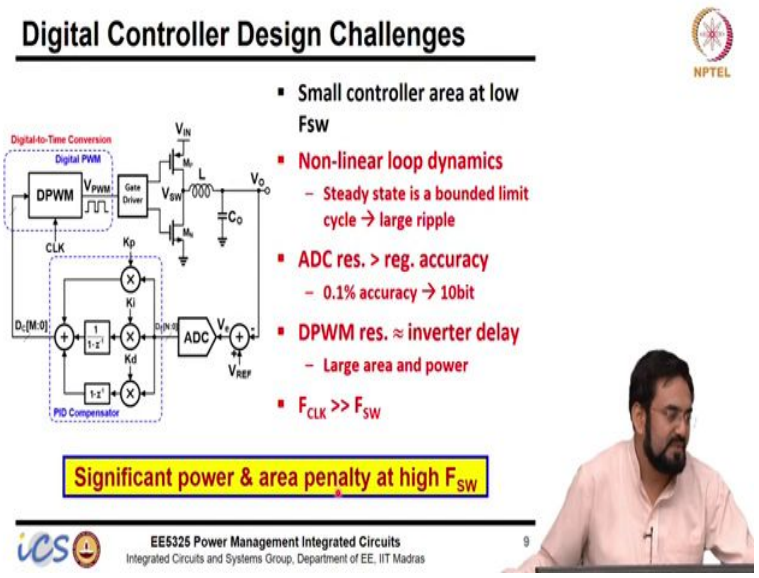
Then for 4 megahertz its 1 microhenry you are using and once you go to 8 megahertz you will be using maybe 0.25 or half of microhenry. Every time you double the frequency, you can do one-fourth of the inductor size. So, at 8 megahertz you can hardly differentiate between your capacitor and inductor. So, that is the reason we want to push our switching frequency as high as possible so that we can achieve a smaller passive size.



But there are some limitations with the analog controller, if I want to increase the switching frequency and I want to still operate at 1/10 bandwidth, I need a very high gain bandwidth error amplifier, I need a very fast comparator because I cannot have a large delay here then basically that will limit my duty cycle if you have a larger error.

So, the same thing with the ramp generator, you require a reset. So, reset will require some time and that time has to be very small compared to your switching period. So, when you are increasing let us say I am running at 100 megahertz then I cannot have 1 nanosecond reset time, it is almost 10 percent of your total time.

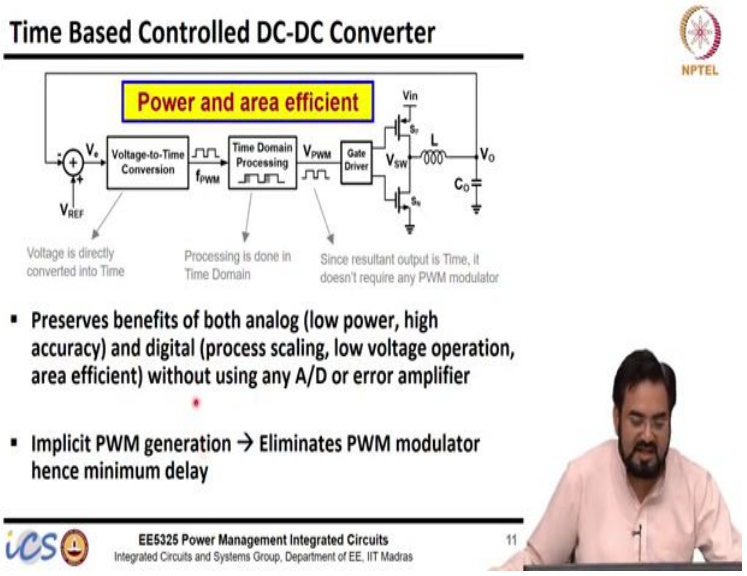
So, it should be a very small fraction let us say even much less than 1 percent comparator again. So, which means everything will contribute to your area here. So, a significant power penalty you have to pay at high F_{SW}.



Then if you are going for a digital controller. So, ADC let us say you want 10 bit and we talked about two cases where one case you can limit the range of ADC, but let us say I am looking for full range then designing that ADC with such a high speed is difficult because I want my ADC output to be available within one cycle.

If you are looking for let us say 100 megahertz kind of a DC-DC converter then the bandwidth of ADC should be much higher. So, you have to incur a lot of area again in the ADC, and if the number of bits are increasing then it becomes even more difficult to design very high bandwidth.

And the DPWM, again let us say you are using DLL then it depends on inverter delays and if I want more resolution then the delay of each inverter should be very small, and then your inverter should be very fast and which means it will take a lot of area and power. So, you are increasing the size of your inverter to make it fast which means you are increasing the power as well as area. So, again here significant power and area penalty you have to pay.



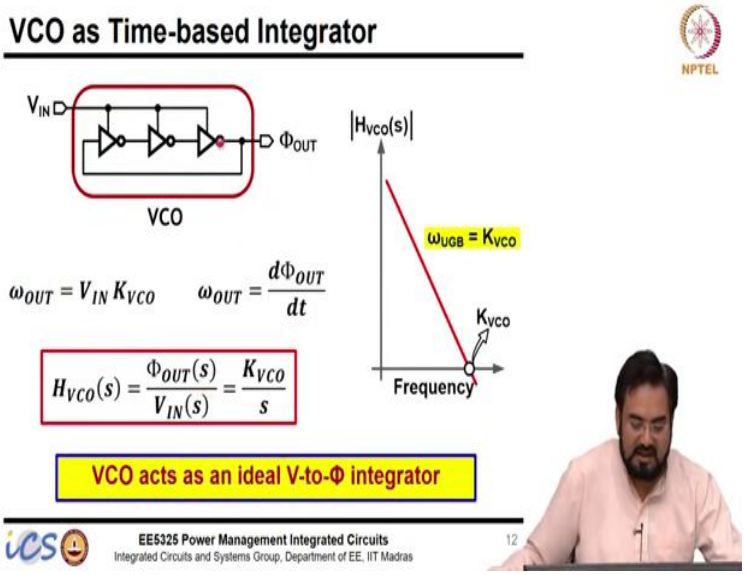
So, then in the time based controller, I am only interested in PWM here and PWM is nothing but a time signal. I am not interested in a level of PWM, the level is getting converted in the power FET. So, I am only interested in the time information here. You take the error signal in a conventional DC-DC converter. If you are using analog, you will be processing in analog voltage signal or if you are using digital then you will convert to digital and then process it. So, in both cases, you are doing either digital processing or voltage processing and then you have to convert that into time by using a PWM modulator.

We are directly converting into time in time based control and we will process everything in time and my resultant will be time. I do not require any PWM modulator here. So, we got completely rid of the PWM modulator. So, it has saved me a comparator, I do not require any ramp and there is no delay associated with that and I can run at higher speed also. So, that is the main advantage. Now it is dealing in the time and not in the voltage levels because I am processing in time. I can run it at any voltage but can I design an op-amp which will run at 1 volt? It is very difficult. If I want to achieve a very high gain, you have to do cascode or gain boosting and it will limit your swing. So, your devices may go out of saturation and it will kill everything but here it is just a time and I am interested in delay.

So, I can run at a lower voltage and we can easily scale with the process also. So, that is the advantage of this. If you look at it after converting to time it is looking more like a clock and the clock is nothing but a digital signal. So, it looks like a continuous time digital basically.

So, it preserves the benefits of both analog which is low power, high accuracy, and digital which is processes scaling, low voltage operation, and area efficient and so we will see that when we process in the time domain, we do not require any capacitor actually. So, let us say for the integrator we required a very large capacitor here you do not require that capacitor at all. So, all those PID compensators can be designed without using any R and C or very small R and C. In some cases, you may require maybe an order of 1 or 2 picofarads only, not like more than 50 picofarads or 100 picofarads we saw in the other case.

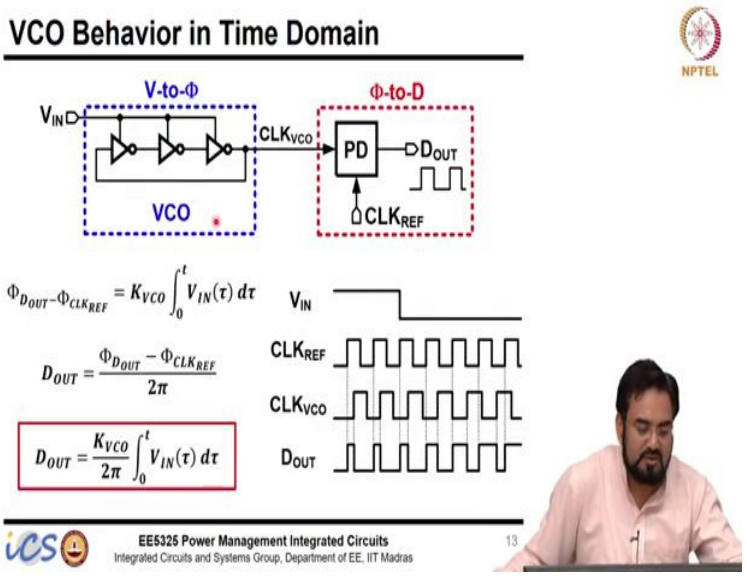
And it has an implicit PWM generation. So, it does not require any PWM modulator. So, we are minimizing the delays associated with your comparator as well as the reset time which you required to reset your ramp.



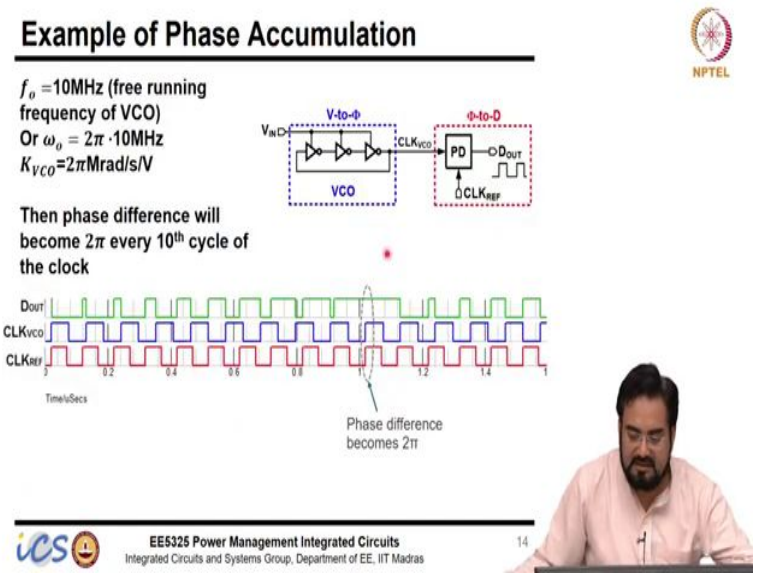
It is highly power and area efficient and we know voltage controlled oscillators. So, ω is dϕ/dt. So, if you want to calculate the ϕ, it will be integral of ω. So, if you give any change in the frequency, it will be integrated into phase and if I am using a voltage controlled oscillator then the frequency is proportional to voltage. So any change in the voltage will get integrated into the phase. So, if I am looking at a phase transfer function which means phase divided by your input voltage it will be K_{VCO} over s where K_{VCO} is the gain of VCO, and people who basically are taking PLL will understand this even better. When you model the PLL, you model the VCO as an integrator.

The VCO is acting as an integrator. So, this simply is like three inverters connected back to back here and output and input is shorted, you get a ring oscillator, and if you can make it a current controlled or voltage controlled whatever it does not matter. So, you get an integrator and you can control the gain by controlling the K_{VCO}.

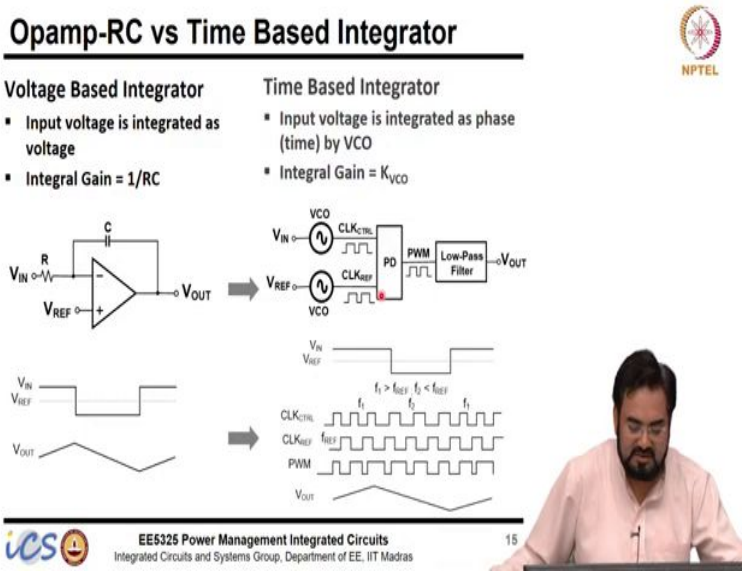
So, without any capacitor, you can get the integration function here and in the PID we require proportional, integral, and derivative.



So, now this is showing the time behavior. So, let us say this is my input step signal. So, when I give a step signal, the clock frequency of VCO will change and if I compare it with the fixed reference then I will get the output nothing but more like a PWM because cycle by cycle phase is integrating. So, every cycle your phase difference between the reference clock and this VCO clock will keep changing and that will get translated into a pulse width. The phase difference is nothing but a pulse width. What do you get here is the duty cycle output.



And this is how your phase gets accumulated. So, let us say this is free running frequency of this VCO and it is 10 megahertz which is 2 pi into 10 mega radians per second, and if K_{VCO} is 2 pi mega radian which is 1 megahertz per volt or 2 pi mega radian per second per volt. The phase difference will become 2 pi for every 10 cycles. K_{VCO} will define how much the phase will change in 1 cycle when you give the step at the input. For every 10 cycles, your phase will become 2 pi and then again it will start. We want to avoid this condition. Let us say maximum you can get a 100 percent duty cycle but the moment you go to 2 pi, it will again go to 0 because the phase will fold back. That is a problem with this actually. You do not allow it to go more than 2 pi otherwise the duty cycle will get reset and your output will die. So, because we do not our duty cycle to saturate to 100 percent. This is called actually cycle slip which happens in the PLL and in converters we call it duty cycle slip because this cycle is corresponding to a duty cycle here. Which means your converter should settle before it goes to 2 pi. Otherwise, you will get a cycle slip and the output will go completely out of regulation.



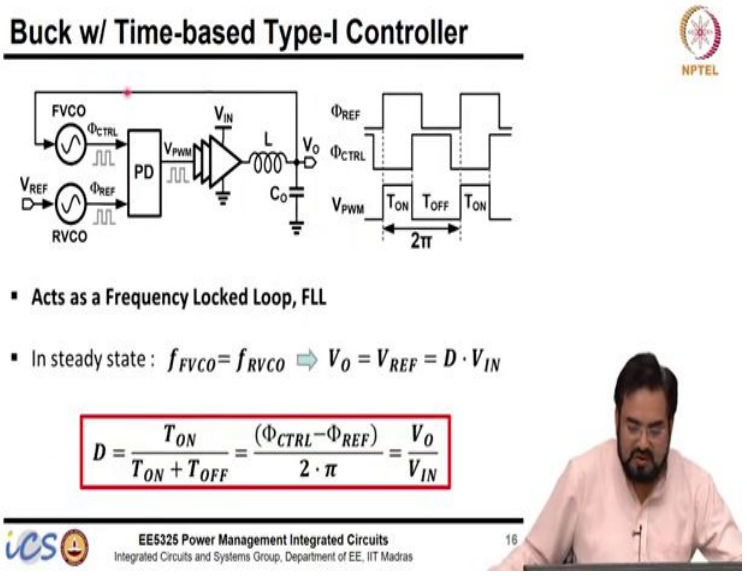
If I compare the opamp-RC and time based integrator, we know that opamp is fully differential at the input and output is single ended. If I have RC, the integral gain will be 1/RC and if I give a square wave at the input, I should get a triangular wave at the output.

Now, I can have 2 VCOs. One is connected to V_{in} and another one is connected to V_{ref}. We can think about this as the positive terminal and this is the negative terminal. Now, this VCO will give me Clk_{ref} and this VCO will give me Clk_{ctrl}. V_{ref} is fixed. So, CLK_{ref} is fixed and V_{in} is variable. So, CLK_{ref} will vary accordingly.

Now, I have a phase detector that will give me the difference between the two phases, and I will get a PWM and pass it through a low pass filter that PWM will get converted to your DC or low frequency signal. So, this filter should have a very low cut off where we can filter out all the ripples at PWM and we can get only the signal frequency.

So, let us say if I put a box around this. I mean input and output. So, let us say this filter is good enough to filter all the ripple, you can hardly differentiate between these two. So, both functionality will be exactly the same. So, the reason we use a VCO for generating CLK_{ref} because if I feed it directly CLK_{ref} then with process voltage or temperature this VCO will change. So, you will not get the same thing in that case. So, we want this guy to track this guy, correct. So, whenever V_{in} is equal to V_{ref}, no matter what is the VCO frequency both will

have a 0 phase difference, provided that your VCOs are matched. You cannot have a different K_{VCO}, otherwise, you will get an offset.



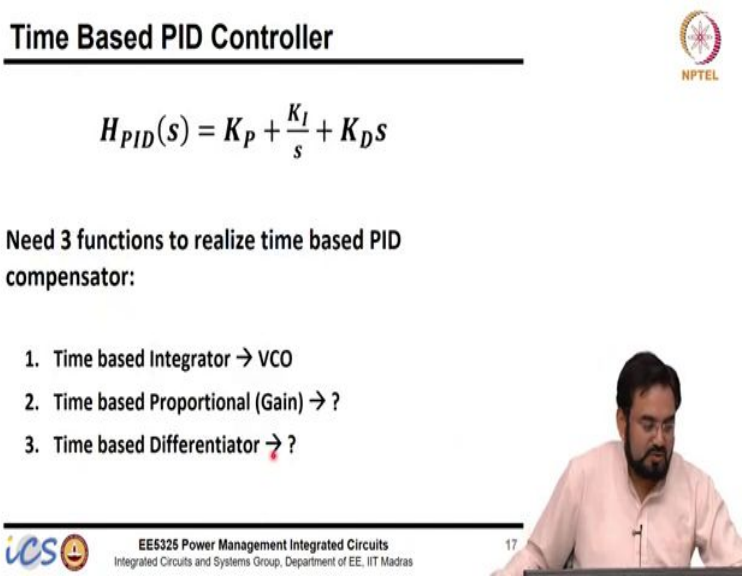
We can easily convert the same thing to type I. In type I, we know the compensator is nothing but an integrator. So, simply you put two VCOs, one is fed by $V_{ref,}$ and the other is with the feedback and if there is any difference between the V_{ref} and V_{out} that will get converted into a phase difference and we will accumulate and we will change that duty cycle. So, the only condition is that VCOs should have the same frequency when V_{ref} is equal to V_{out}.

And if I want V_{ref} equal to V_{out}, the duty cycle here should be corresponding to V_{out} over V_{in}. Let us consider no loss. Even in feedback if there is a loss then it will compensate for that. So, which means it will always lock in frequency and I am not locking the phase here, I am only locking the frequency. So, the phase is free to go anywhere because I want a different duty cycle. If I lock the phase and make the phase difference between these 0 then I will always get a 0 percent duty cycle which will not help me.

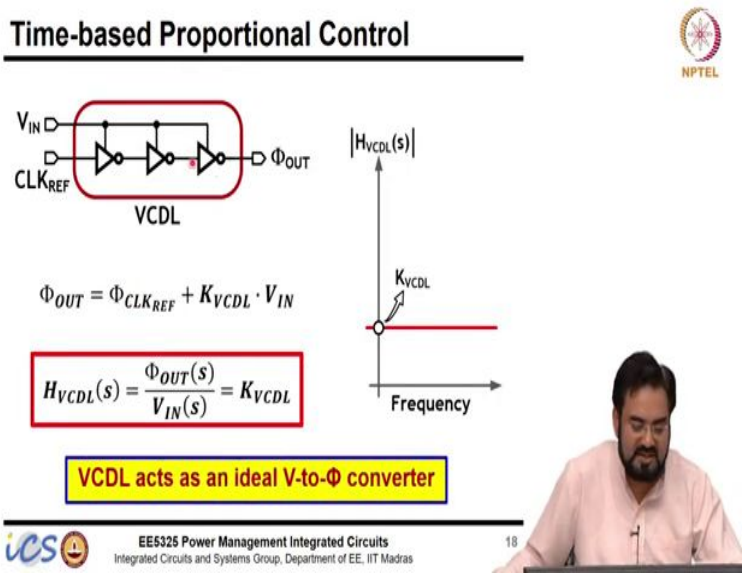
So that is why I do not want to lock phase but only lock-in frequency so that my phase is free to go anywhere and it will always lock at the duty cycle which will give me the desired output or V_{out} equal to V_{ref}. So, this will be your D, now D you can relate with the phase difference. So, the phase difference between these 2 divided by 2 pi will give you the duty cycle, just like we do T_{on} over T_{on} plus $T_{off,}$ and in the voltage domain, your duty cycle is

nothing but V_{out} by V_{in} and if you have a voltage controller or analog controller your duty cycle is V_{ctrl} over V_m.

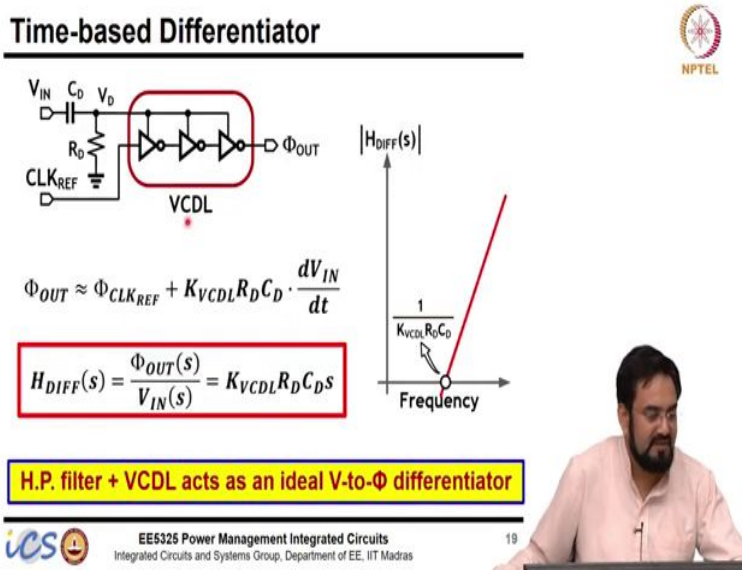
So, you can assume here this ϕ_{ctrl} minus ϕ_{ref} is nothing but it is phase representation of your V_{ctrl} in phase domain and 2 pi is representing your amplitude of your V_m, here amplitude is of the phase is 2 pi. So, everything is now you are looking in the x direction rather than y direction.



So, type 1 is easy. We only need VCOs but now if I want to do PID then for PID we need both proportional and derivative. We already know how to do it. So, we need to implement time based proportional and time base differentiator.

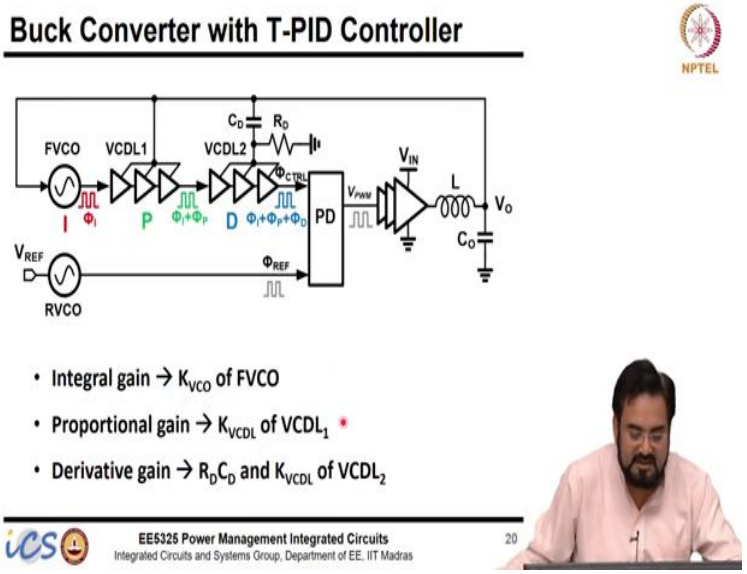


So, proportional is just like we have VCO we have VCDL(Voltage Control Delay Lines), where your delay will be proportional to V_{in} and delay is nothing but a phase. So, there the phase was integral of input here phase is directly proportional to the input. So, it is looking more like a gain, Φ_{out} equal to K times V_{in}. So, if you look at a transfer function it will be the gain of this VCDL which is K_{VCDL}. So, you will get a flat curve here but implementing a derivative component is not easy.



So, what do we actually do for derivative? We simply put a first order low pass filter and use the same VCDL. So, if the RC time constant is small enough to push that pole outside. So, it will behave like a differentiator.

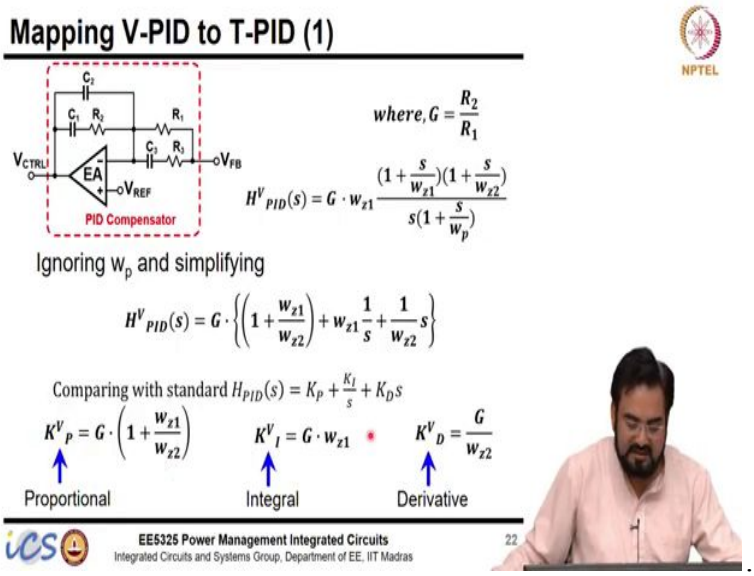
So, your pole is outside the UGB. So, you will get only s term in the numerator. The denominator is out of the picture. So, then VCDL will give me the gain. So, I can use it as a derivative component and it will give me this kind of behavior; basically, the zero at origin just like an integrator gives me a pole at the origin. So, which means high pass filter plus VCDL acts as an ideal voltage to phase differentiator.



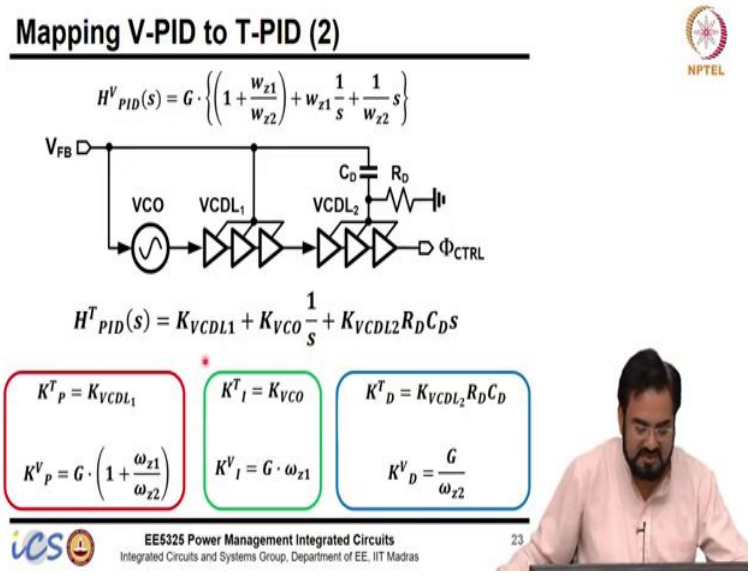
So, now we have all three components and we know that delays are added when you cascade them. So adding them is not difficult, just keep cascading. So, this is my integral. Now, VCDL1 is proportional then with the high pass filter another VCDL gives me the derivative component.

So, if this is a Φ_i, this is Φ_p, Φ_i plus Φ_p because the input to this is Φ_i. So, input to this is Φ_i plus Φ_p. So, the output will be Φ_i plus Φ_p plus Φ_d. So, this Φ_{ctrl} will have all the three components integral, proportional, and derivative. Now, you can use this reference VCO again with V_{ref} and the feedback will always force the duty cycle to give me the desired output.

So, the only thing now you have to decide how you design these VCDL K_{VCO}. So, that you can place your zero and make your loop gain according to your requirement.



So which means first we have to do voltage mode. We know how to design the voltage mode where to place the zero and pole, because from here it is very difficult to say where is the zero and where is the pole, but here we can easily tell. We always look in terms of poles and zeros. We never look in terms of K_i, K_p, and K_d, it becomes very difficult. You cannot understand that until and unless you know the zero. So, those zeros can get converted to K_i, K_p, and K_d and we know how to convert that. Our integral and derivative component in terms of 0. If you remember this was the equation we came up with earlier. So, once we do not know those zeros we can easily calculate K_i, K_p, and K_d and we already have and I think we already discussed how to break this into those three components. So, you have to basically ignore the pole and divide by s. So, you can get that K_i, K_p, and K_d.



So, we know the K_i, K_p, and K_d in this and all we have to do is just relate this one with the other. So, in the time domain your proportional is nothing but K_{VCDL} and K_i is nothing but K_{VCO} and K_d is K_{VCDL2} into R_D C_D which is the high pass filter actually and in the voltage domain in terms of zero this is this and if we equate them we know ω_{z1} and ω_{z2}, we can calculate K_{VCDL}, K_{VCO}, R_D, and C_D. We can calculate and map to that and model in the frequency domain and design the whole thing.