Power Management Integrated Circuits
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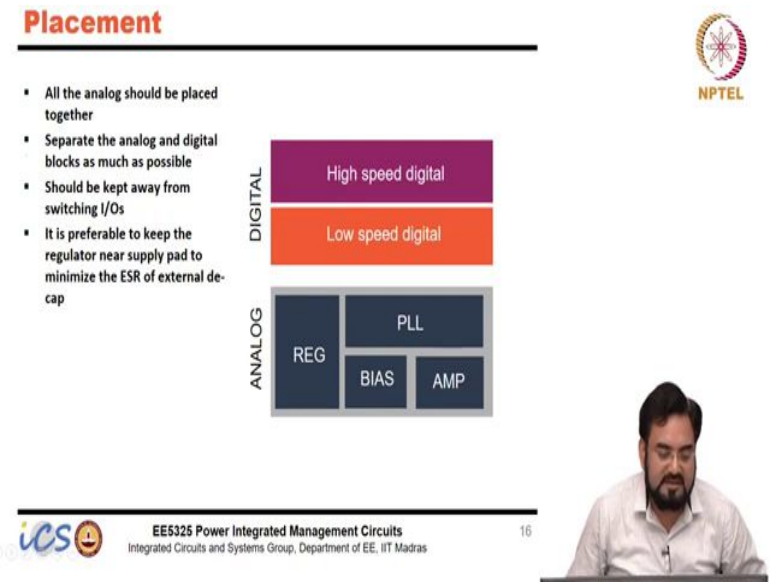
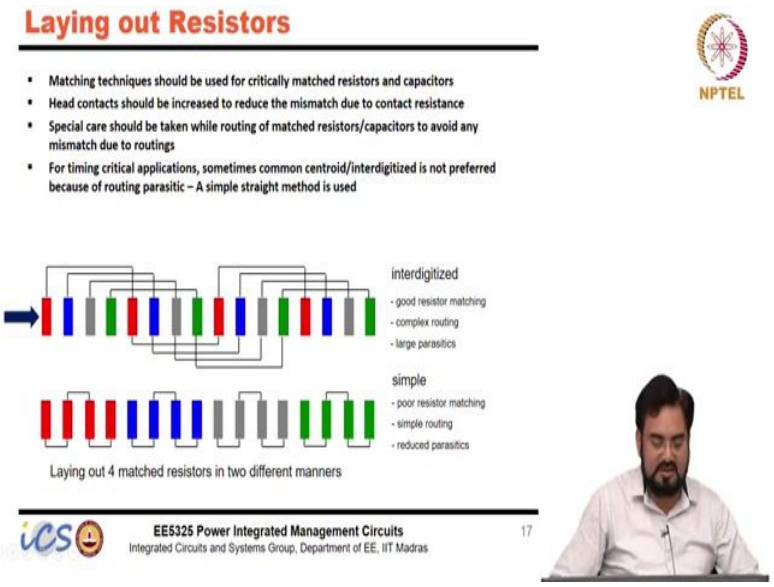
Lecture – 91
Analog Layout Techniques - Part 2

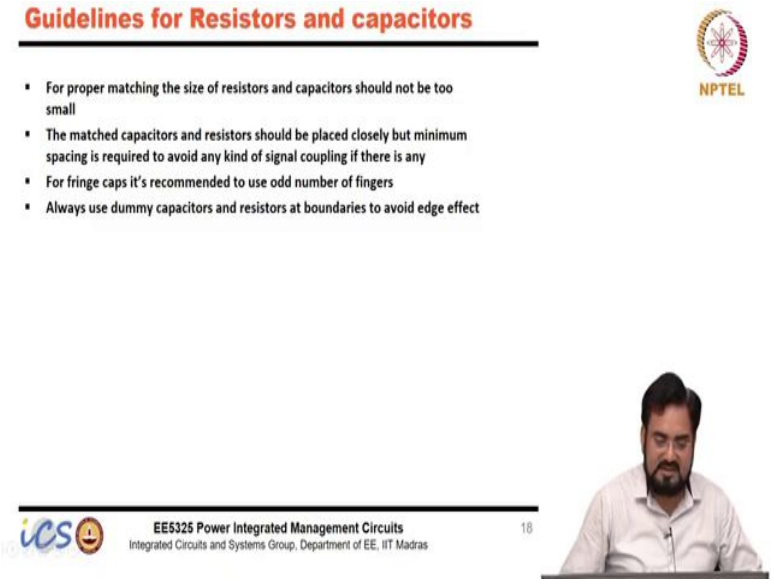


All the analog should be placed together. Most of the time we have on any chip both analog and digital components. We try to keep the digital and analog separate. All the digital components should be placed together and all the analog components should be placed together. And we try to maintain some spacing, do not keep them very close otherwise again noise will get coupled from digital because it's switching and it may corrupt your analog signal.

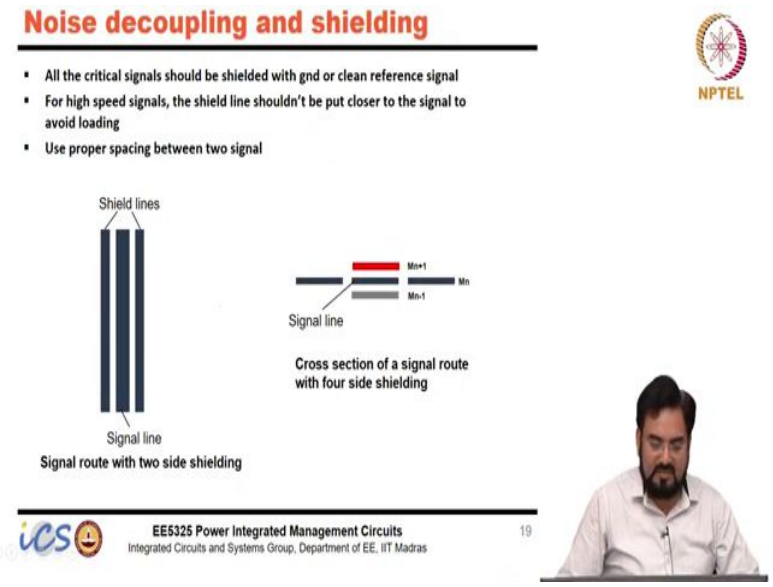
So, that is why we always try to separate them out and there are some guard rings and all those techniques we use to have better isolation.



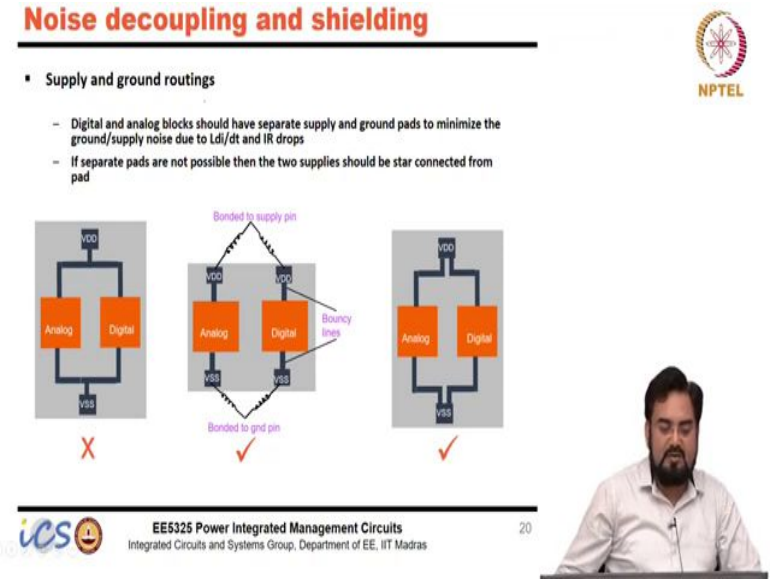
The above image shows two laying out techniques for laying out resistors. In interdigitized, we get good resistor matching but routing is complex and complex routing may introduce resistor parasitics. In simple routing, parasitics are reduced but we get poor resistor matching. If resistor value is large compared to parasitics then we can use interdigitized but if parasitics are even 1 percent of the resistor value then it may introduce problems in some applications.



Guidelines for resistors and capacitors layout are shown in the above image.



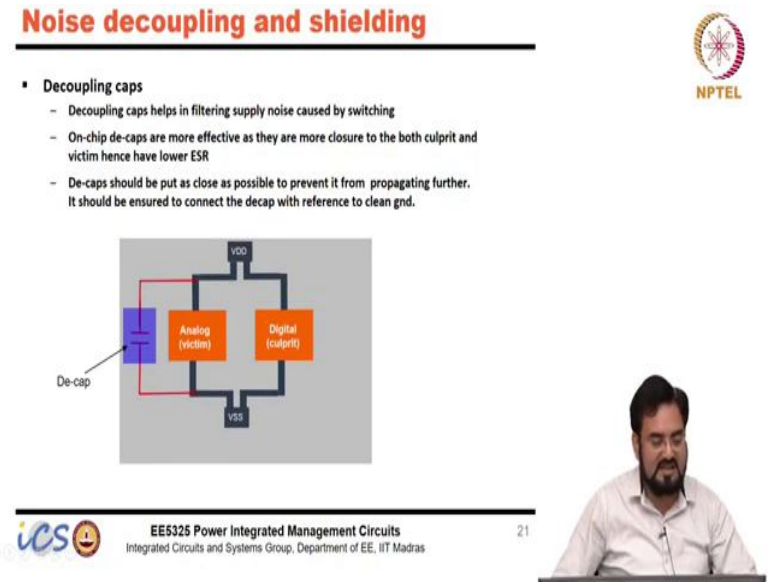
Noise decoupling and shielding. So, what happens if we have a critical signal then. For example, we are routing a reference, and we have a lot of digital signals going around it. We do not want that digital to get coupled to your reference otherwise it will create some noise. So, we create a shield on all 4 sides and connect it mostly with the clean ground or any clean reference. So, that in between the shield we have the reference, and if let us say on the other side you have any clock going on, so your shield will block that.



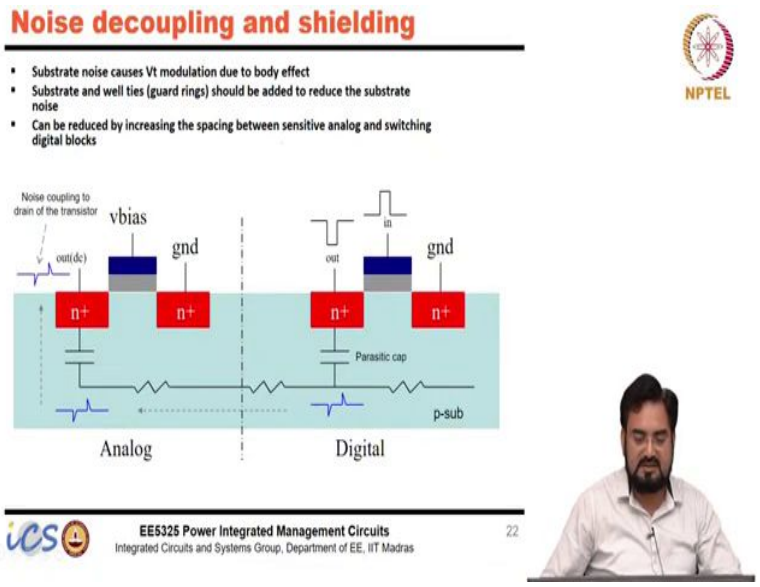
Supply and ground routings are very important. So, if we have analog and digital blocks then do not short their supply and ground routings locally and then have a single metal connected

to the pad. Always try to connect in star form as shown in the above image or if we have the option of multiple pads then the best thing is to have separate pads for them.

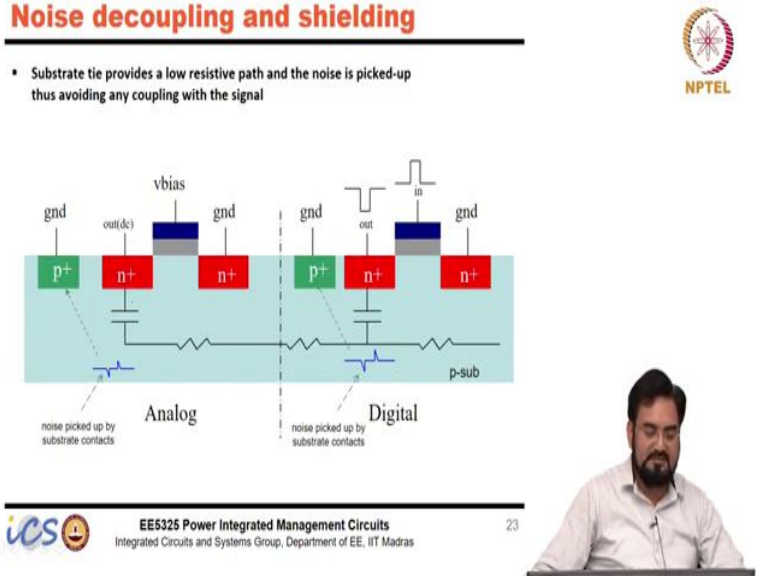
When we connect the source directly and route them separately then the chances of coupling between analog and digital are less but when we connect supply and ground routings locally then there we have created an additional resistor between the connection of routings and pad and now the signal can couple from digital to analog and corrupt circuit.



Decoupling cap so, always try to use a decoupling cap and that should be placed closer as close as possible to the module. The reason is we want to decouple the noise close to the analog block and if we connect far away then we will add resistance, and then it will look like ESR in the capacitor and that will not be a very effective capacitor. So, always try to place your decoupling cap closest to the module not away from the module. This is just showing how the noise gets coupled.



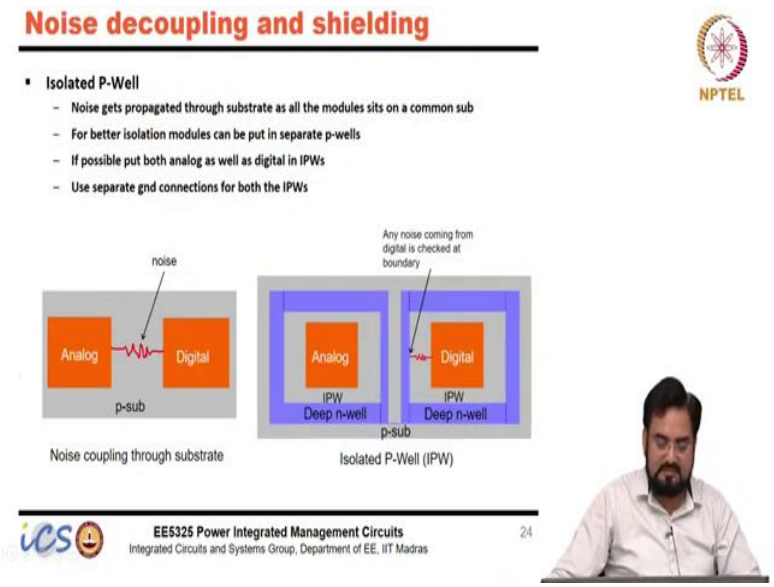
We use a lot of guard rings. The guard ring is nothing but the contacts and diffusion put around your well and substrate. So, digital si switching and we always have a capacitor between this source and bulk that we already know these are parasitic caps. And if the digital signal is switching then the parasitic capacitor will couple the noise and inject it into the substrate; and this can propagate through the substrate and picked up by the analog block. This can be reduced by increasing the spacing between sensitive analog and switching digital blocks.



Best way to remove the noise is to create a low resistive path that can pick the noise signal before it reaches capacitor. So, what we do we put substrate contact and connect it to ground.

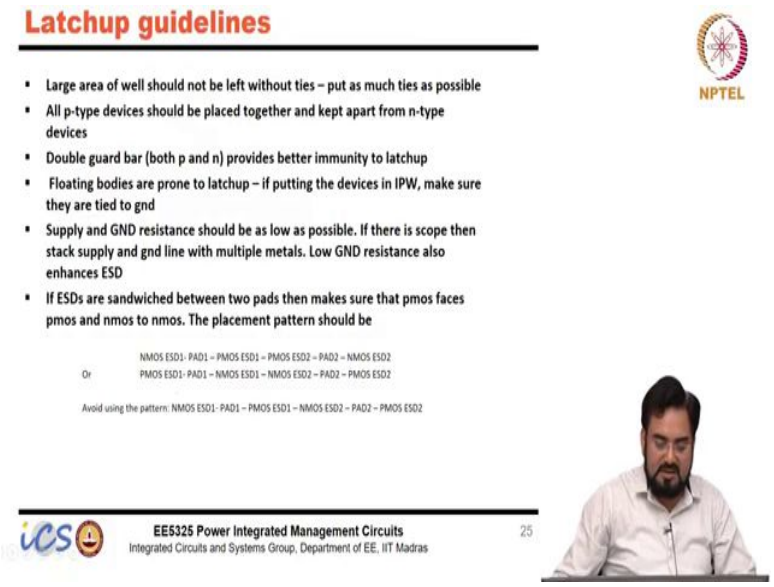
Substrate contact will create a low resistive path between gnd and substrate and this will pick up the noise and remove it before it reaches the signal.

And that is why we use these diffusions or guard rings on both the device. So, depending upon whether NMOS or PMOS. So, if it's a PMOS then it's created in N well and contact is N+ and if it's a NMOS then it's created in P well and contact is P+. In case of N-well, we connect the contact to the Vdd and Vdd will pick up the noise.



Isolated P-well so, some process have an option where you can isolate both analog and digital block. So, if the substrate is common which means digital and analog both are sitting in the same substrate then noise can travel from one susbtrate to another substrate. So, if I want better isolation I can build them in a separate substrate completely different.

So, there is no connection between the two as you can see in the above image for isolated P well case. So, there is something called deep N-well and what deep N-well is nothing, but you put a bowl of N-well; that goes deep down and there is something called buried layer inside at the bottom. So, you vertical wall you create on both the sides and then the bottom and this is nothing, but the N type diffusion. So, your P is completely carved out of that. You create another P-well inside the P substrate. So, this is called isolated P-well. If you have this option then always try to utilize this and keep analog and digital in separate P-well.

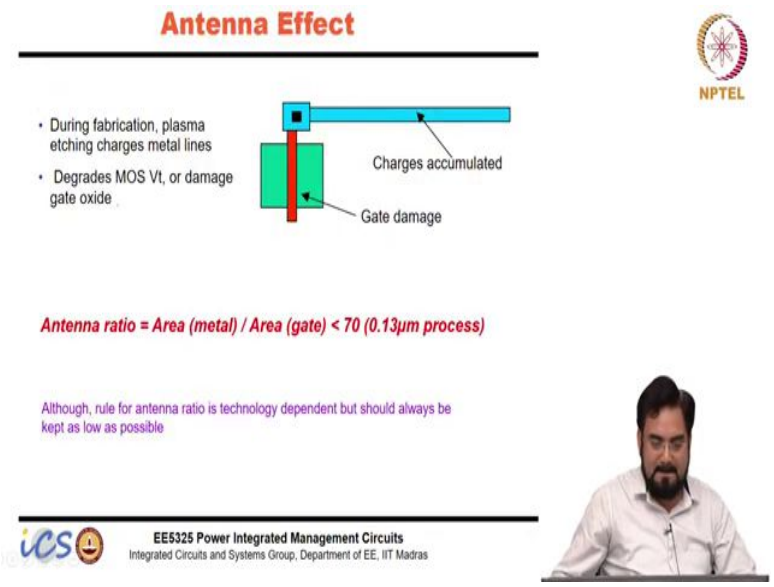


Latchup guidelines are shown in the above image. We have all N-type P-type diffusion and it creates a PNP NPN junction and that becomes a parasitic bipolar. So, back to back bipolar it creates more like a latch kind of a circuit, and if one of the bipolar turns on then it will create a short between Vdd and ground and that is called latchup.

So, the best way to reduce the tendency of latchup is to separate out the devices. And mostly latchup is created when both N channel and P channel place together if you have all P-type and N-type then it would not happen. So, those 2 by bipolar are created between an NMOS and PMOS just like an inverter in the inverter we have both NMOS and PMOS. So, the tendency of latchup in the inverter is high if both N and P are placed together.

In the electrostatic discharge sensitive device (ESDs) we most of the time use NMOS and PMOS devices. When the chips come back if we connect our finger or any surface actually it can discharge the charge to the pin and the gate cap is very small.

The voltage created on that pin will be very high like the order of Kilo volts. So, that can puncture the gate and that is why we use ESDs. ESDs what they will do they will basically take all the charge and dump to the ground before it reaches the gate. We have to make sure that all the N-type and P-type transistors are side by side in ESDs and not put nmos and pmos together because that may have a more tendency for latchup.

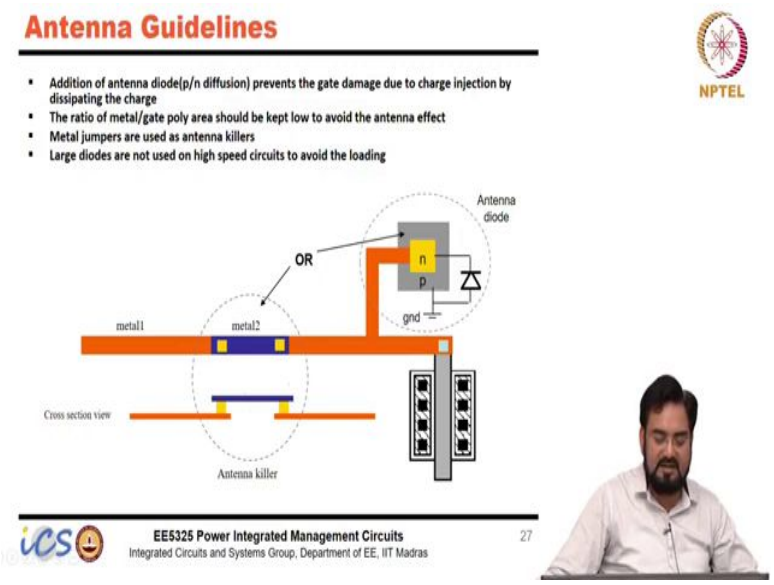


During fabrication, plasma etching charges metal lines, and these charges can dissipate to the gate and they can alter threshold voltage(V_t). Those charges will get trapped in the gate and they will alter V_{th}. Let us say it happens on one gate and it does not happen on the other gate in diff pair then the V_{th} of the two devices will be different and it will create offset and we can never get rid of this offset without using offset cancellation techniques.

We always try to reduce this as much as possible and do not fully depend on offset cancellation techniques and use them only as a secondary precaution. And we know that dynamic cancellation is not applied everywhere. If we have a continuous comparator or continuous-time Op-amp then we may have a ripple problem at the output if we do dynamic cancellation.

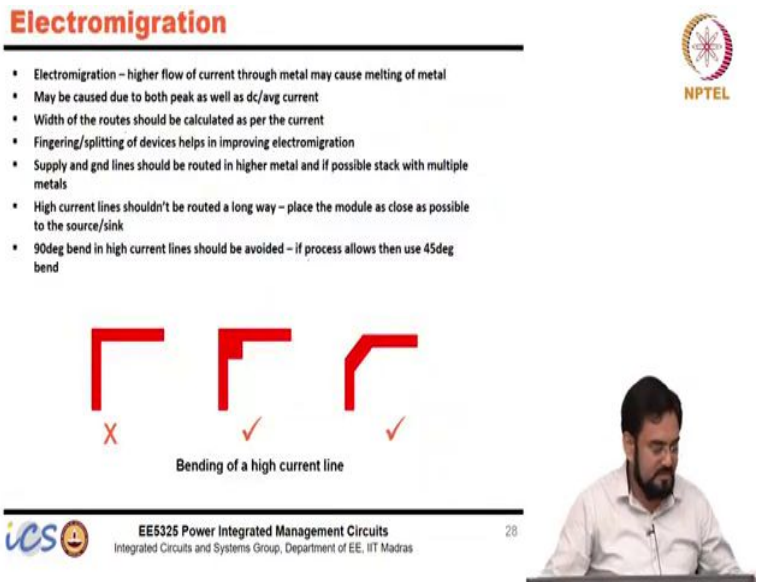
The technology files when we design our chip and layout, it will have some antenna rule which is called the Antenna ratio. So, the area of metal over the area of the gate should be less than 70. Let us say this is for 0.13 micron process. This means if we put a large metal on a small gate, then the tendency of this antenna effect is more compared to a small because this large metal means the area of metal is more then it will have more charge.

So, I want to simply reduce that charge so, one way like you can affront try to make sure that this metal's area is not enough, but in case let us say you have routed a long way the area is long; the area is large then we put antenna diode.



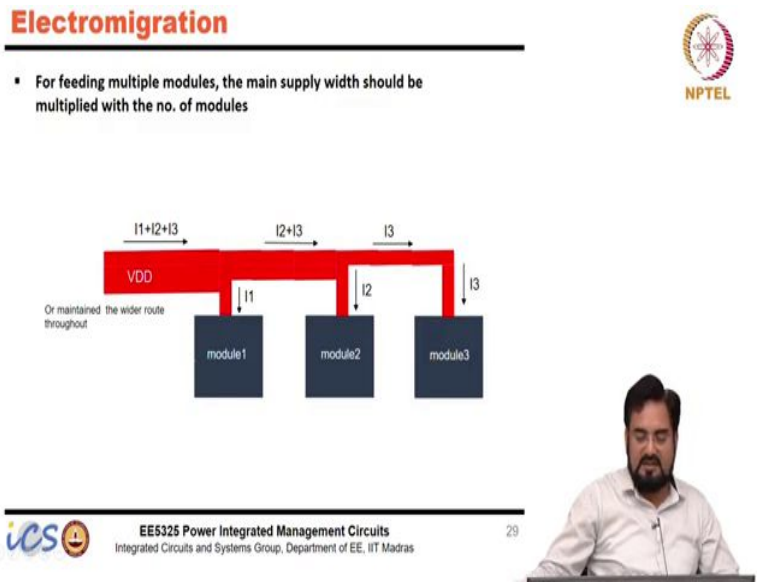
Structure of Antenna diode is shown in the above image. Addition of antenna diode(p/n diffusion) prevents the gate damage due to charge injection by dissipating the charge. Whenever we have a diffusion then it would not create a problem, the problem is created when we have a gate because it's insulated and there is no path for the charge.

There is another technique called jumper or antenna killer. what we do instead of routing in a single metal we route in multiple metals. Structure of antenna killer is shown in the above image. Strips of metal 1 are not connected When the metal 1 metallization is done on the first layer. So, the gate will see only one portion, it will not see the other portion when you do the metal 2 then this is small all the charges will be on metal 2 only metal 1 will not have any charge that time. So, that is how you create. We reduce the area of metal by breaking them into different layers that is it. Both techniques are valid, we can use any of them.

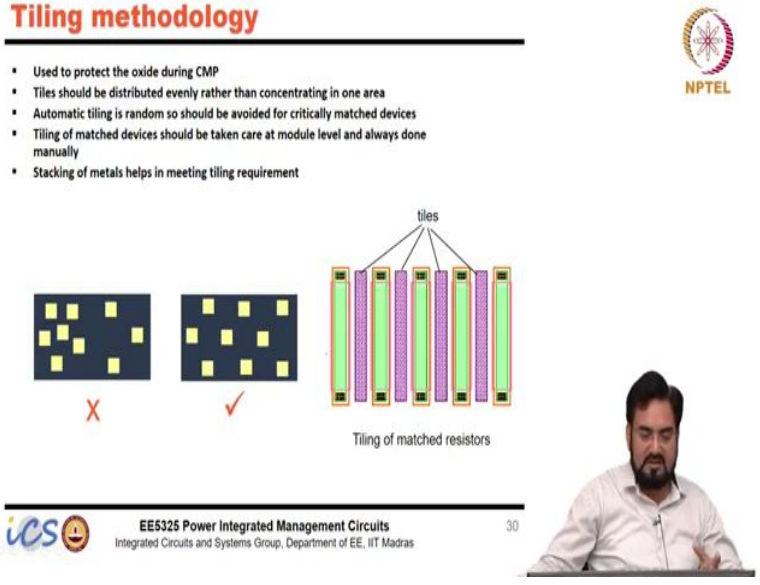


Electromigration is when higher flow of current through metal may cause melting of metal. We have to make sure that the metal line the width of the metal should be enough to carry the required current. All the process technologies have rules for maximum current per unit width can carry and most of the time we have different specifications at room temperature and maximum temperature. Always design for max temperature, and on top of that keep margin because the electromigration if it occurs it will melt and your chip is dead.

When we have a 90-degree bend then basically the effective resistance at the corner will be much higher compared to straight wire. We put a patch at the corner or have a 40 to 45 degree bend as shown in the above image.



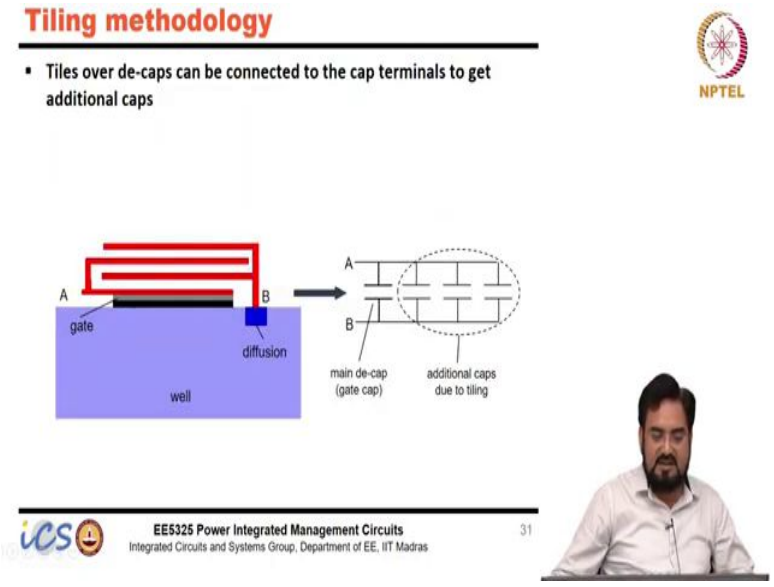
For feeding multiple modules, the main supply width should be multiplied with the no. of modules. An example is shown in the above image. We have to make the width based on how much current is flowing or make the width uniform based on the maximum width required for the safest operation.



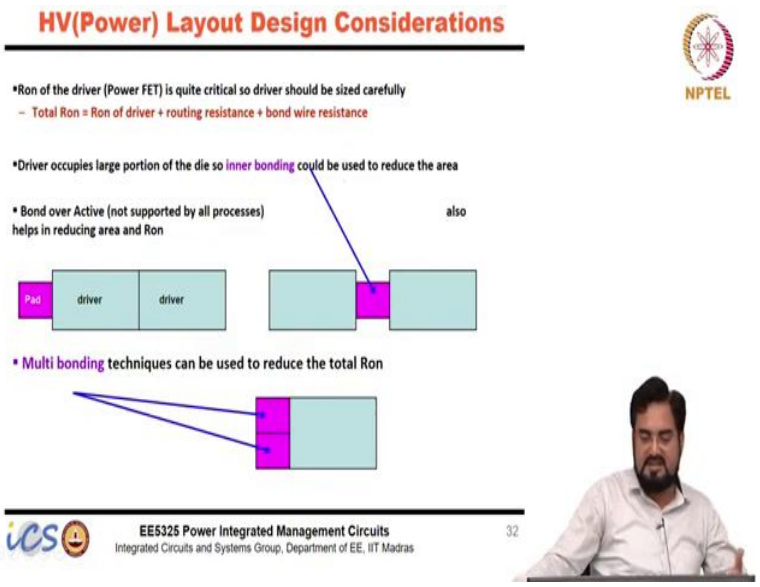
The base oxide layer is soft and can be damaged during CMP. If there is no metal during polishing then base oxide can be damaged. We should minimum metal density according to the requirement of technology. In digital blocks, we generally use automatic tiling in which it will run a script that will randomly put tiles to pass the density rule. But in the analog block,

if matching is required then we cannot randomly put tiles to pass the rule because it will affect the matching and we have manually put dummy blocks to pass the density rule.

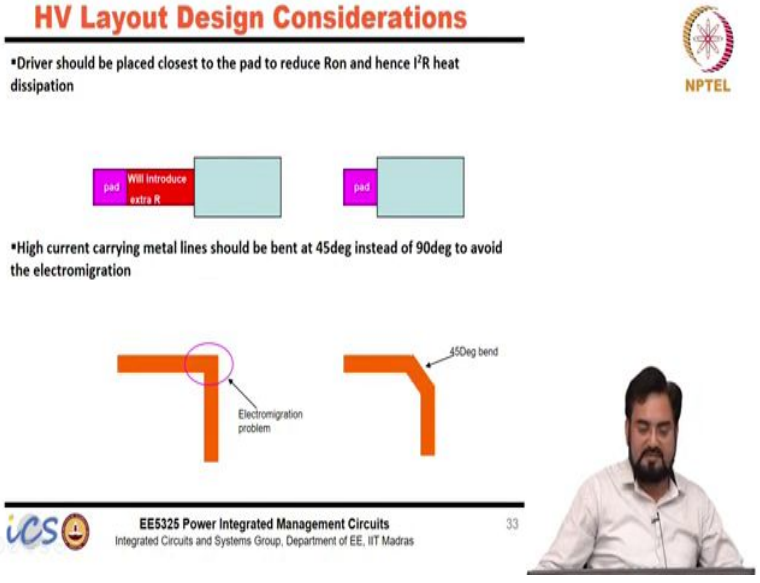
When our chip goes in the top level for integration where they have both analog and digital then they will try to integrate the module with this. So, what we do there is something layer called anti tile layer or tile block layer where you. So, you match the density rule for your meet the density rule for your block and put that tile layer. So, that when they put the tile on the top level they will not touch your module; otherwise it will affect the matching.



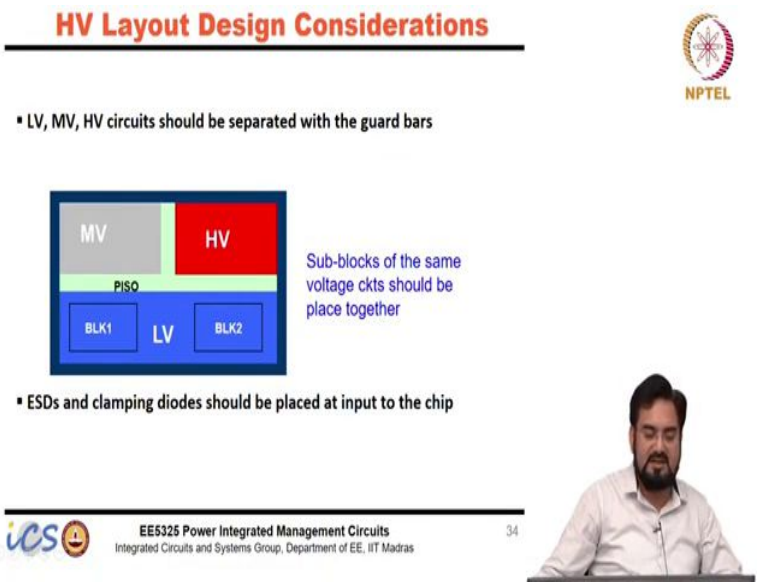
We can use tiles over our gate caps for getting the extra cap. Example is shown in the above image.



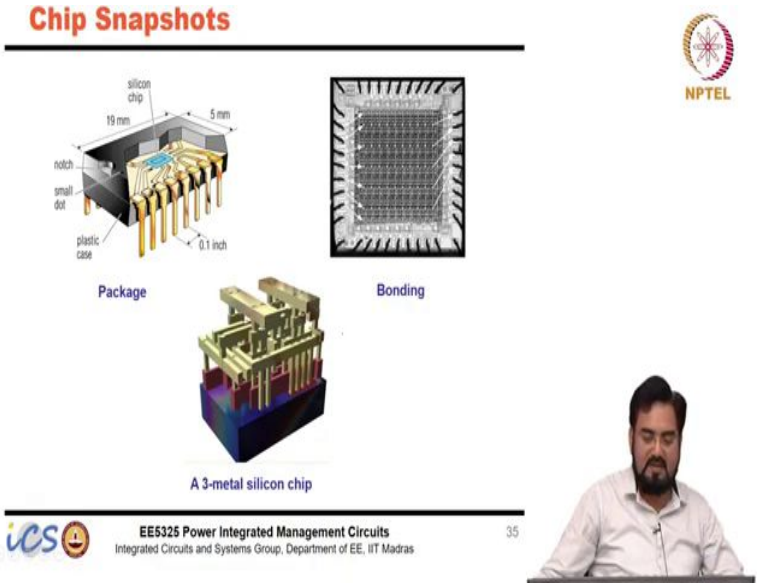
In High voltage layout design consideration, we try to reduce the routing distance to reduce the IR losses. If we have a high voltage and high current routing and have 2 power FETs then we do not put the pad on the one side either put them like on top of the other and use double bonding or put the pad in the center.



We always try to use 45 degree bend if the option is there and if it's not there then try to increase the width at the corner and always put the pad closer to the device do not route it longer because that will introduce IR losses.



If we have multiple voltage devices then always try to isolate them with the guard bars or guard rings.



The above image shows the chip snapshots. So, the package is usually much bigger compared to die size until unless we are using the WLP package. WLP is a wafer-level package where the package size is the same as the die size. 3D view of a 3-metal silicon chip is shown in the above image.