

Power Management Integrated Circuits
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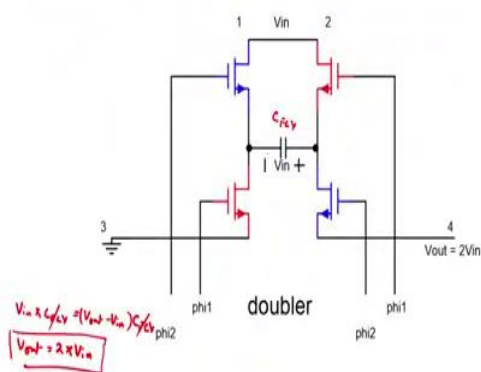
Lecture – 88

H-Bridge Switched-Capacitor DC-DC Converter, SC DC-DC Converter with Multiple Gain Settings

So, what do you need to do? You have 4 switches across one flying cap and depending upon where you connect V_{in} and V_{out} that so, you short if these 1 and 2. So, there are 4 terminals 1, 2, 3, 4.

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H-bridge Topology - Boost



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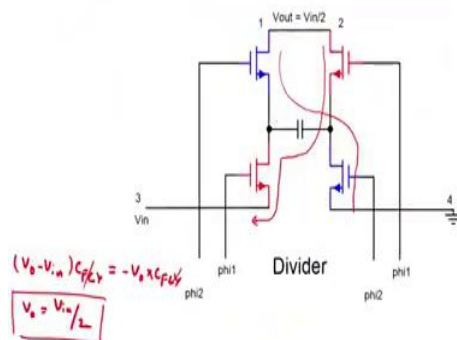
So, if you short 1 and 2 and apply V_{in} here and on the other 2 switches, one is connected to ground in one phase and other is connected to V_{out} in the other phase then so, what you are doing actually you can see, what is happening during this phase 1. So, this is your phase 1 right. So, during phase 1, what is the charge across this capacitor?

V_{in} into C_{FLY} so, V_{in} into let us call it C_{FLY} equal to what is the charge across this capacitor during phi 2?

So, this gets cancelled out. So, what do you get V_{out} 2 times V_{in} ok.

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H-bridge Topology - Buck



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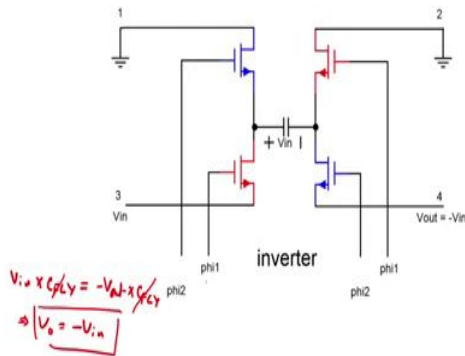


Now, let us look at the buck, this is half V_{in} by 2. So, now, it is exactly the, I mean flipped version of this. Now V_{in} becomes V_{out} correct and V_{out} becomes V_{in} and ground remain same correct. If you remember the how we converted a buck into boost we just flipped the input output. So, it is similar situation here so, let us see so what is happening in phi 1?

What is the voltage across this capacitor phi 1? During phi 2 and this is phi 1 ok. So, during phi 1 what is the charge? V_{out} minus V_{in} into C_{FLY} equal to look at the other phase. Because in phi 1 your charge is in this direction and your phi 2 the other plate is actually connected to V_{out} . So, that is why it is a minus. So, again this gets cancelled out and your V_{out} is V_{in} by 2.

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H-bridge Topology - Inverting



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Let us see the inverting case. So, during phi 1 what is the charge? Let us say this left hand side is plus, then V_{in} .

So, now, if I want to divide by 3 how can I do that? See if I want any other ratios I know the charge remains the same if the capacitor remains the same they cancel, they are cancelled out, but nobody is forcing you to have the same cap during phi and phi bar you can have a different caps ok.

So, let us see how we do V_{out} equal to V_{dd} by 3. If you look at the voltage across this capacitor that will be equally divided so, this will be V_{dd} minus V_{out} by 2 and this would be. So, Q is how much? V_{dd} minus V_{out} by 2 multiplied by C_{FLY} .

So, Q total is twice of because we have 2 capacitors here and when you connect in parallel the total charge will be added. So, you can think of like you have 2 buckets and when you pour both the buckets in another cap. So, you will get a $2 \times$ charge.

So, each cap charge of each across each cap will get added when you dump on the output capacitor sorry ok. Now during this phase let me move this, we have a twice cap; now 2 into C_{FLY} multiplied by V_{out} .

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$V_o = V_{dd}/3$

during ϕ

$\frac{V_{dd}-V_o}{2} \times C_{FLY}$

$Q = \frac{V_{dd}-V_o}{2} \times C_{FLY}$

$Q_{total} = 2 \times \frac{V_{dd}-V_o}{2} \times C_{FLY} = (V_{dd}-V_o) C_{FLY}$

$Q_{total} \text{ during } \phi = Q_{total} \text{ during } \bar{\phi}$

$V_{dd}-V_o = 2V_o \Rightarrow V_o = \frac{V_{dd}}{3}$

during $\bar{\phi}$

$\frac{V_o}{2} \times C_{FLY}$

$Q_{total} = 2 \times \frac{V_o}{2} \times C_{FLY} = V_o C_{FLY}$



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$V_o = V_{dd}/3$

during ϕ

$\frac{V_{dd}-V_o}{2} \times C_{FLY}$

$Q = \frac{V_{dd}-V_o}{2} \times C_{FLY}$

$Q_{total} = 2 \times \frac{V_{dd}-V_o}{2} \times C_{FLY} = (V_{dd}-V_o) C_{FLY}$

$Q_{total} \text{ during } \phi = Q_{total} \text{ during } \bar{\phi}$

$V_{dd}-V_o = 2V_o \Rightarrow V_o = \frac{V_{dd}}{3}$

during $\bar{\phi}$

$\frac{V_o}{2} \times C_{FLY}$

$Q_{total} = 2 \times \frac{V_o}{2} \times C_{FLY} = V_o C_{FLY}$

iCSC

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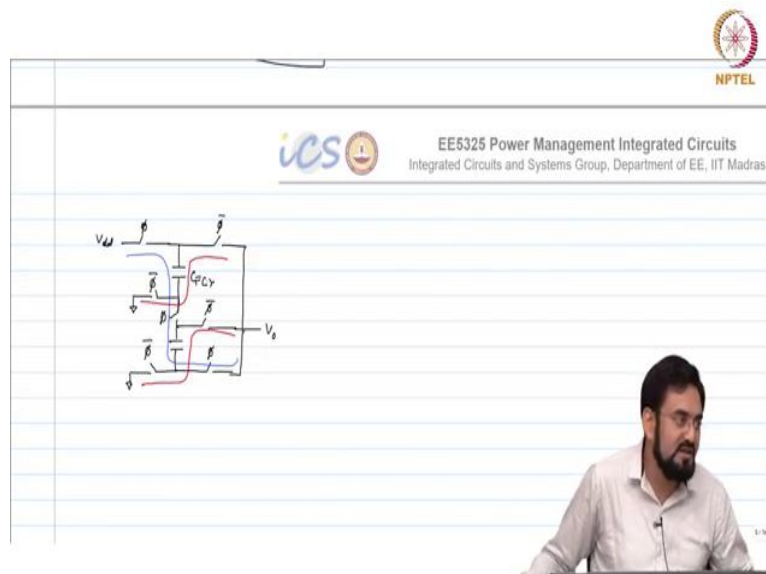
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So, which means Q total during phi equal to Q total during phi bar equal to twice of V out which implies V out equal to V dd by 3.

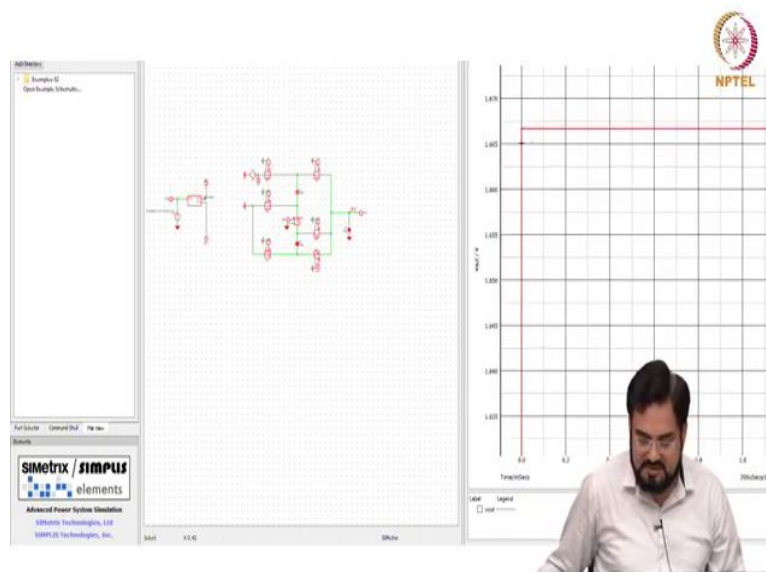
So, you can do V dd by 4, V dd by 5 by connecting more capacitors, but it will require more switches. So, if you want to exactly implement this, then let us see how it will be V dd C FLY, let us say this is phi bar.

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So, during phi this switch will be on so, this is on, this is on and this is on. So, these 2 capacitors will come in, so let me draw like this is, this is the actual path ok. So, the voltage across these 2 capacitors will be V_{dd} minus V_{out} and they will be in series.

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Now, let us see during phi bar. So, during phi bar we need 1 more switch here. So, this will get connected to the output phi bar and this will be grounded. So, one capacitor between V_{dd}

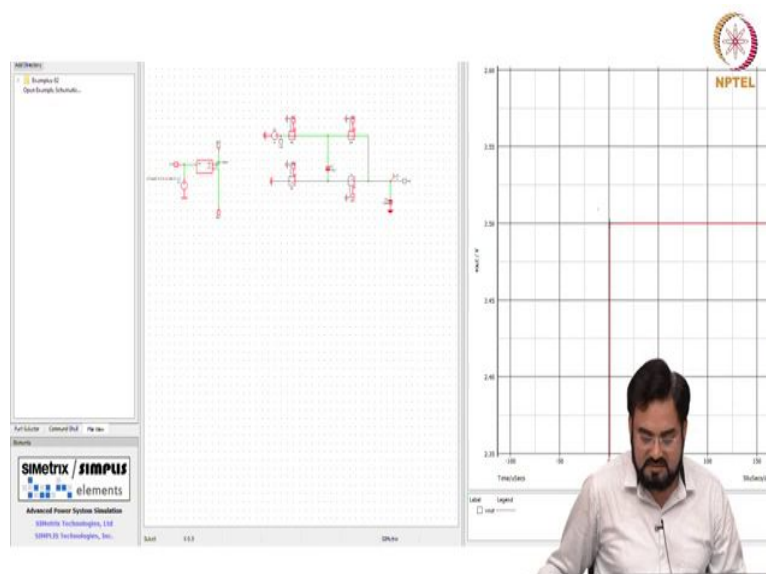
out and ground and this will get connected to V_{out} and this will be grounded. So, both will come in parallel ok.

So, you will get this configuration. So, this is your one and the second one is this. So, if I want to do let us say V_{dd} by 4, you can do in the same manner or another option would be you already know how to do V_{dd} by 2, you can cascade the same and you will get V_{dd} by 4.

So, whichever gives you smaller number of switches and smaller number of capacitors you can opt for that? So, and you already know V_{dd} by 2 will requires only one capacitor. So, if you cascade them the total number of capacitors will be 2 and if you do V_{dd} by 4 here, you need one more cap. So, obviously, the number of capacitors looks smaller and hopefully the number of switches will also be less because 3 capacitors will require more switches compared to 2 capacitors. So, this same structure 2 capacitors and those switches are connecting in the series and parallel.

So, I have 5 volt input. So, your output should be one third of that. So, 1.67 so, it is one third ok, this divided by 2. So, you get 2.5 volt usually this is how you do, you have to basically make a parallel and series combination in ϕ and ϕ bar and get a different ratio so that you can get different output voltages.

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(5) Improved eff. design because $I_L = I_{load}$ (buck)

Regulation Volt in DC de-dc converter

$V_{in} = 12V$

$V_o = 5.8V$

C_{fb}

R_f

I_{load}

R_L

$V_{fb} = 1.2V$

Clock generator

Clock

en

V_{fb}

$V_o = \frac{1.2}{0.5} = 2.4$

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So, as we look ah, looked into this regulated charge pump; if you remember and if you do not regulate at its gain, so let us say I have done a 2 x charge pump. But my output to input ratio is not 2 x, but let us say 1.5 x or something then your efficiency will drop ok, because you are not allowing your charge pump to settle.

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NPTEL

V_{FB}

$1.2V + \Delta V_{FB}$

$1.2V - \Delta V_{FB}$

t_{on}, t_{off}

$\Rightarrow$ Similar to PWM operation in inductive load

In open loop

$V_o = 5V, V_{dd} = 2.5V \rightarrow$ efficient

$V_o = 3.3V, V_{dd} = 2.5V$ (closed loop) $\rightarrow$ inefficient as $5V - 3.3V = 1.7V$ will be dropped.

η

94%

60%

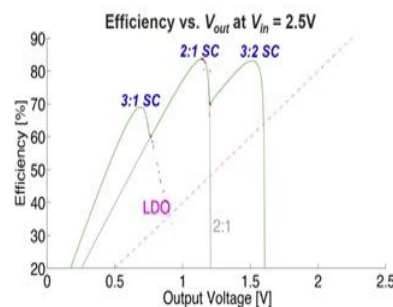
1.6V V_{dd} 2.5V

So, if I want to cater to a wide range of voltages V_{out} over V_{in} then you need multiple ratios ok.

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Efficiency of SC DC-DC Converter

- Efficiency peaks $V_o/V_{in} = \text{Gain}$
- More gain settings are required to achieve higher efficiency across wide V_o/V_{in} range $\rightarrow$ flatter efficiency curve



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If you do not have multiple ratios what will happen? So, this is your LDO actually. So, let us say my V_{out} is here I think V_{out} is 1.2 volt or so, and V_{in} is 2.5 volt correct.

So, for half 1 by 2, 1.25 volt so, if your output is varying. So, here you need roughly one by third. So, 2.5 by 3 is roughly 0.8 volt or so, this is the point where your dropout is maximum which means LDO will have very bad efficiency. But if I have a charge pump which can do one third; then you can see efficiency is much better, but now if I move away from this ratio then you can see efficiency is dropping.

So, I would like to operate this charge pump always at its gain, not away from it, so let us see if I am operating away from it and I do not have this 2 is to 1, if I do not have 2 is to 1 what would happen? It will keep going like this ok, efficiency will keep dropping, but when I am moving away what I did actually I switched to 2 is to 1.

So, now efficiency will improve and when I have a half which is roughly 1.25 volt your efficiency will peak again and it will start dropping when your output voltage is increasing. So, if I do not have, let us say 1 is to 2, I mean I do not have this other 3 is to 2 ratio, then it

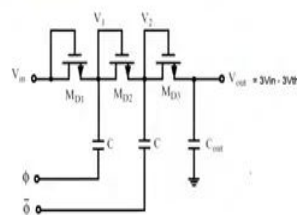
will keep dropping efficiency. But I have a 3 is to 2 so, I will switch to that and then again. So, by having more gain settings I can have basically.

High efficiency across a wide range of input output voltages or you can say output to input ratios. So, it is not necessary that output is changing, output may remain fixed and input is changing. So, it is the same thing actually it is just a V_{out} by V_{in} ratio ok. So, that is the advantage of having multiple gain settings.

So, usually what you do, you have multiple switches and you configure the switches based on which gain settings you want to go. So, just like we looked at one H-bridge architecture this can be configured in $2 V_{dd}$ and V_{dd} by 2 and V_{dd} , also V_{dd} is nothing, but it is a bypass mode.

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Basic Concept



- Step 1- $\phi = 0$
- $V_1 = V_{in} - V_{th}$
- Step 2- $\phi = V_{in}$
- $V_1 = 2V_{in} - V_{th}$
- Step 3- $\phi = 0$
- $V_2 = 2V_{in} - V_{th}$
- Step 4- $\phi = V_{in}$
- $V_2 = 3V_{in} - 2V_{th}$
- $V_{out} = 3V_{in} - 3V_{th}$



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So, you just short V_{in} and V_{out} . So, we can configure it in 3 settings. Forget about the negative voltage, let us say we always want let us say positive voltage. So, we can have 3 settings with this depending upon how you configure the switches ok.

So, which means more gain settings will require more switches and it may require more capacitors, also let us say if I want V_{dd} by 4 or V_{dd} by 3 then you may have to connect the

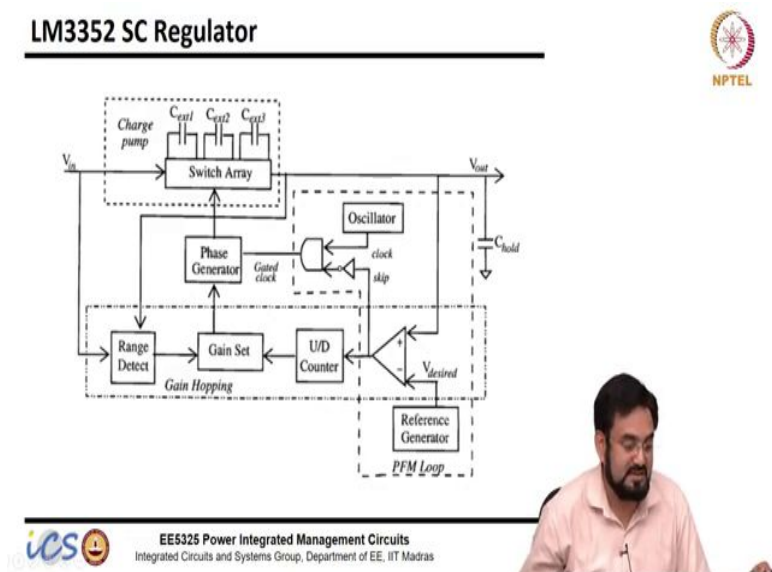
capacitors in series and parallel to get final ratio then you may require more capacitors also and more switches.

So, as you keep increasing the gain settings and make it very high resolution your complexity will increase and you may not be able to achieve the same efficiency because your switches will have loss $CV^2 f$ loss, then your conduction loss will also increase because in series, there will be multiple switches connected.

So, everything will contribute to loss and your efficiency will decrease, but overall average efficiency will look better. Your peak efficiency may drop so let us say if I had only one setting. So, instead of this 70 percent, it may be looking at 80 or above 80 percent. If you have only one settings, but in the same switch capacitor converter I have multiple settings.

So, you may drop 5, 10 percent, but on an average you can say efficiency will be looking better compared to an LDO or compared to a single setting switching converter, the switch capacitor switching converter ok.

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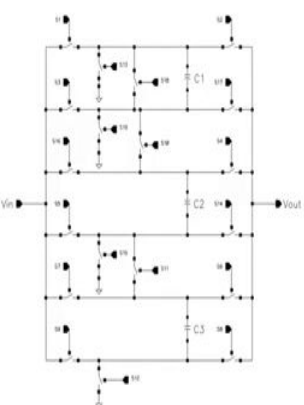


So, this is a product actually LM 3352 from TI and it has multiple settings and you can see that they have a switcher here and all these capacitors are external. So, they are having 3 capacitors here and V_{out} is the C_{hold} is here. So, all 3 are flying capacitors ok.

So, they can be connected in parallel and series depending upon the switch configuration and they are also regulating the output with this ok. So, they have a gain setting. So, if you remember, we talked about how you control the gain setting ok. So, you can have a comparator and your accumulator or up down counter and that code will decide basically what gain settings you need to have.

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LM3352 SC Regulator - Switches



Region	Max. Gain	Min. Gain
1	2/3	1/2
2	2/3	1/2
3	3/4	2/3
4	1	2/3
5	1	3/4
6	1	1
7	4/3	1
8	3/2	4/3
9	2	4/3
10	2	4/3
11	2	2

Buck

Bypass

Boost



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So, now in the buck mode they have this 1 by 2, 2 by 3, 3 by 4. So, 3 almost 4 settings if you include 1 also and 1 is a nothing, but bypass so, they have different regions like in the first region they go from maximum gain 2 by 3 to half in the second region 2 by 3 to half. So, these 2 regions are same in the third region they go from 3 by 4 to 2 by 3 fourth region 1 to 2 by 3 and sixth region is nothing, but bypass and then after that they start boosting.

So, you can see how many switches are used here with the 3 capacitors 1, 2, 3. So, they have too many switches. So, they can be connected in series and parallel. So, are like more than 10 switches, here like 13, 15, 17 yeah looks like 19 almost 20 switches.

So, I mean there is a trade-off between like; obviously, whether you want to maintain the average efficiency or you are looking for the peak efficiency if you are only interested in one gain setting then you can do.

So, and we already talked about in what case we are interested only in one gain setting, we talked about cascaded switching regulator and switching inductive switching and switch capacitor if you want to convert 10 volt to 1 volt. So, you can divide by 2 using the switched cap and then do a buck. So, same thing you can do with the LDO also.

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The slide displays two circuit diagrams and their efficiency calculations:

Top Diagram (Standard LDO):

- Input: $V_{dd} = 2.5V$
- Output: $V_{out} = 1.2V$
- Dropout Voltage: $V_{drop} = 1.3V$
- Efficiency: $\eta \approx 50\%$

Bottom Diagram (Cascaded Regulator):

- Input: $V_{dd} = 2.5V$
- First Stage: $\frac{1}{2}$ SC divider, output $1.25V$
- Second Stage: LDO, output $1.2V$
- First Stage Efficiency: $\eta = 91\%$
- Second Stage Efficiency: $\eta = 96\%$
- Total Efficiency: $\eta_{total} = 0.91 \times 0.96 \approx 88\%$

So, let us say I have this LDO V_{dd} is 2.5 volt and V_{out} is let us say 1.2 volt. So, what is the efficiency? Close to 50 percent. Now if I do this. So, what is this 1 point? 25 and then LDO so, dropout is only 50 milli volt here. And what is the V_{drop} here? 1.3 volt. Huge difference, so let us say this guy is 90 percent efficiency not difficult to achieve with a single gain setting. So, what is the efficiency of this regulator 1.2 divided by?

96 percent, so, what is total efficiency 0.9 into 0.96? How much? So, 50 percent versus 86 percent huge difference and if you are looking for very low current, let us say order of 1 milli amp or so, then these capacitors can be integrated on chip then you do not require, but this guy is the I think load current is they are maximum catering to 200 milliamp or so. So, which is impossible with the on chip capacitor so, that is why they are using external.