Power Management Integrated Circuits
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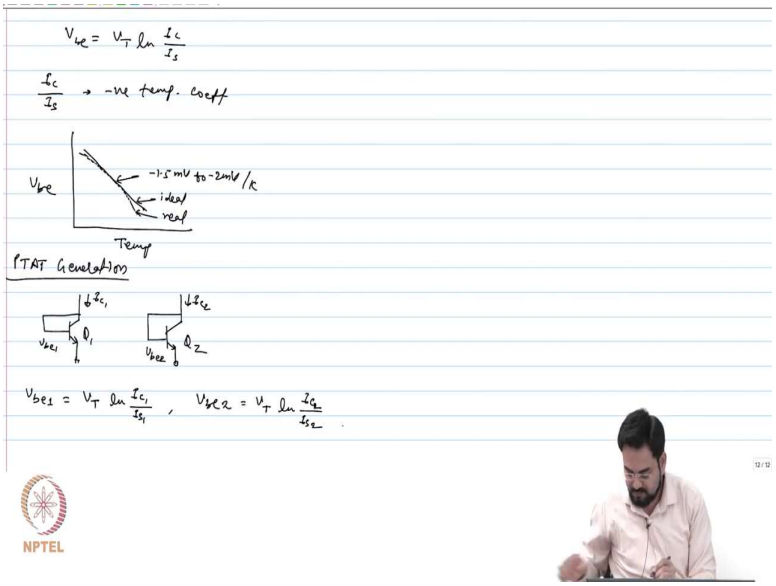
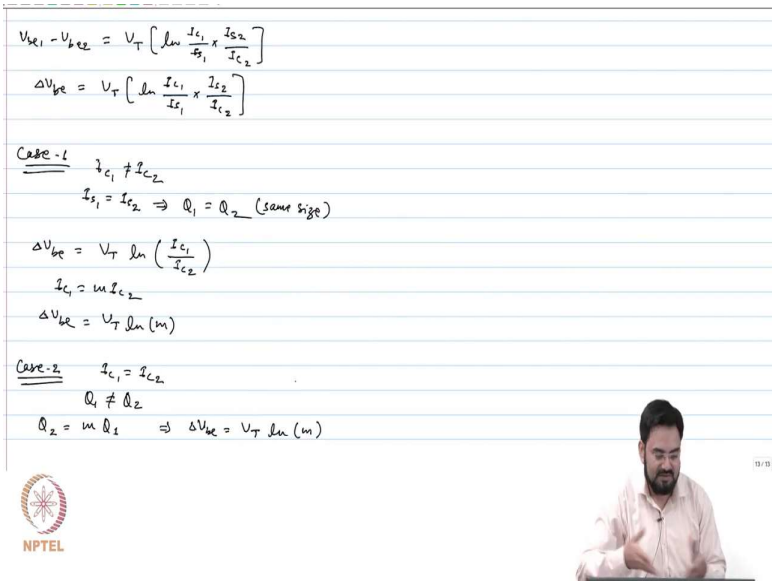
Lecture - 08
Adding PTAT and CTAT voltages

PTAT generation: We know that collector current (I_c) of bipolar is given by

$$I_c = I_s\, e^{V_{be}/V_T} \quad \Rightarrow \quad V_{be} = V_T \ln \frac{I_c}{I_s}$$



Now V_{be} difference (ΔV_{be}) is given as $\Delta V_{be} = V_T \ln \frac{I_{c1} I_{s2}}{I_{s1} I_{c2}}$.



In order to generate V_{be} difference (ΔV_{be}), we can have 2 situations as shown in above figure.

Case 1: Have different collector current for Q1 and Q2 with same size.

Case 2: Have same collector current for Q1 and Q2 with different size so that your I_{s1}, I_{s2} can be different.

Most of the time we use this case-2. So, we always make I_{c1} equal to I_{c2} because this gives us more accurate results compared to the other one. So, we rely only on the difference between the reverse saturation current (I_s) by introducing the area difference between the transistors.

So, now you can change the area or you can change the currents in the 2 bipolars and you can change the slope and get the bandgap. Since it is coming as "ln" term which means m required might be quite large. I mean you can just do the calculation, in order to get a 2 mV slope from 86 µV.

$$86\ \mu V \times \ln(m) = 2\ mV$$

$$\ln(m) = 23$$

$$m = e^{23}$$

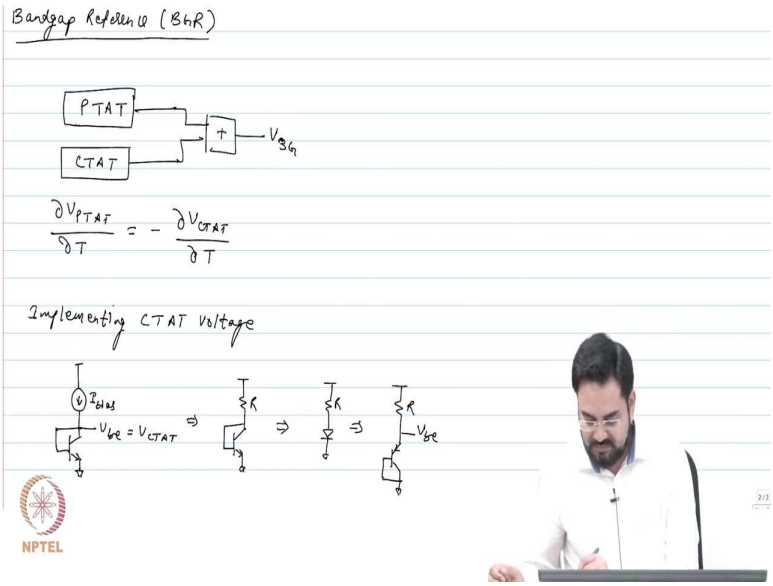
m is quite large, which means your area will be bloated. So, usually we try to keep this m factor small and introduce another proportionality factor. Let us say m you may choose 10, so the size of one transistor will be 10 times of the other.

And then have another proportionality factor by modifying your circuit in such a way and that can be done through resistor divider. So, let us say with this $V_T \ln(m)$, I have another factor which is $\frac{R_1}{R_2}$. Now, you change the $\frac{R_1}{R_2}$ ratio and get the required slope.

In order to generate bandgap, we need one voltage which is proportional to temperature and another voltage which is inversely proportional to temperature. And if we have same slope with opposite sign then they will cancel out and you will get the output as constant across temperature.

V_{CTAT} implementation:

If you connect your bipolar in a diode connected manner it will give you V_{be} and we know that V_{be} is inversely proportional to temperature. And the circuit diagram is shown in below.



And most of the time we use PNP because in the standard CMOS process we get the parasitic bipolar and you do not get active bipolars.

There is a difference between parasitic and active; active bipolar is basically fabricated through the process and it is mostly vertical actually. And you get the parasitic bipolar by default when you fabricate the PMOS and NMOS. So, by default you get the p-diffusion, n-diffusion and p-diffusion.

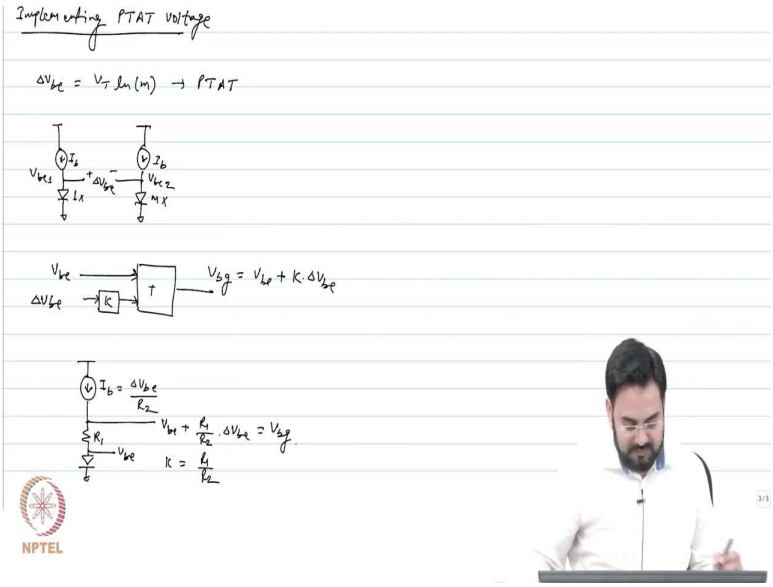
So, three diffusions you get and all three make your collector, base and emitter and you get basically a PNP device. And since this collector is built on P-type substrate and substrate is mostly grounded. So, you get a bipolar by default whose collector is grounded or connected to substrate. You do not have a freedom to connect the collector anywhere else, but you have to ground it.

So, base is N-type here, and if you tie the base to the ground then we get the same diode behaviour. So, the difference between active and parasitic is the gain (β) actually. The β of parasitic bipolar is very bad compared to the active. Active may have β like more than 100 or so, bur these parasitic bipolar may have β much less than 10 or so.

That's why mostly we use these substrate PNPs in order to design the bandgap for a standard CMOS. But if you have a process which has active bipolar then you are free to use. In my circuits I will draw the diode instead of drawing PNP or NPN. So, by default you understand that you have to replace that with a diode connected NPN or diode connected PNP.

V_{PTAT} implementation:

Circuit diagram is shown in below figure. And the V_{be} difference (ΔV_{be}) can be used as PTAT.



But slopes are different, so you need to scale that. So, V_{be} is fixed and V_{be} can't be scaled but ΔV_{be} needs to be scaled to match the slope of your V_{be}. Let's say ΔV_{be} needs to be scaled by K. So, we get

$$V_{bg} = V_{be} + K\,\Delta V_{be}$$

So, V_{be} is straight forward and we have to see how to generate the scaled down version of ΔV_{be}.

One possibility could be instead of taking the difference of two voltages, first I will generate the current $I_b = \frac{\Delta V_{be}}{R_2}$ and dumb into the resistor as shown in above figure.

So, now we get $V_{bg} = V_{be} + K\,\Delta V_{be}$ where $K = \frac{R_1}{R_2}$.