Power Management Integrated Circuits
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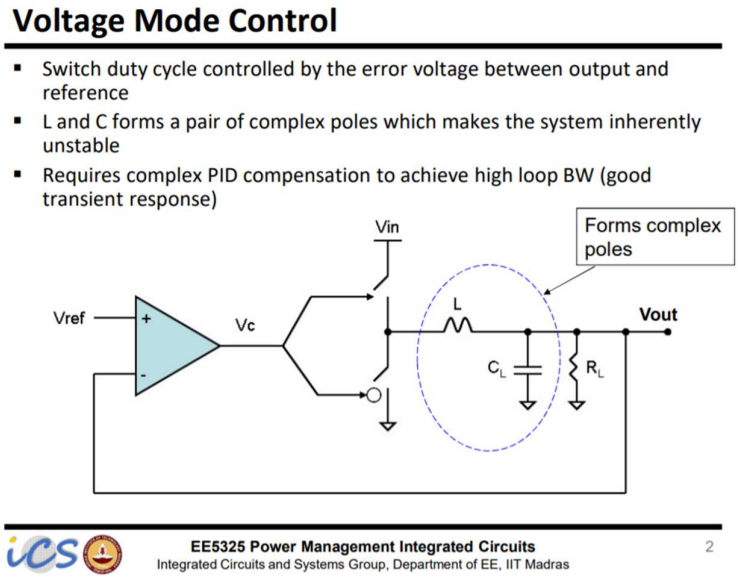
Lecture – 72
Current Mode Control: Peak, Valley, Emulated; VMC versus CMC; Sub-Harmonic Oscillations

So far, we talked about Voltage Mode Control. Now I will briefly give an idea about current mode control. But we will not go in as much detail as we talked about voltage mode control.

Simplified diagram of your voltage mode control is shown in below figure.

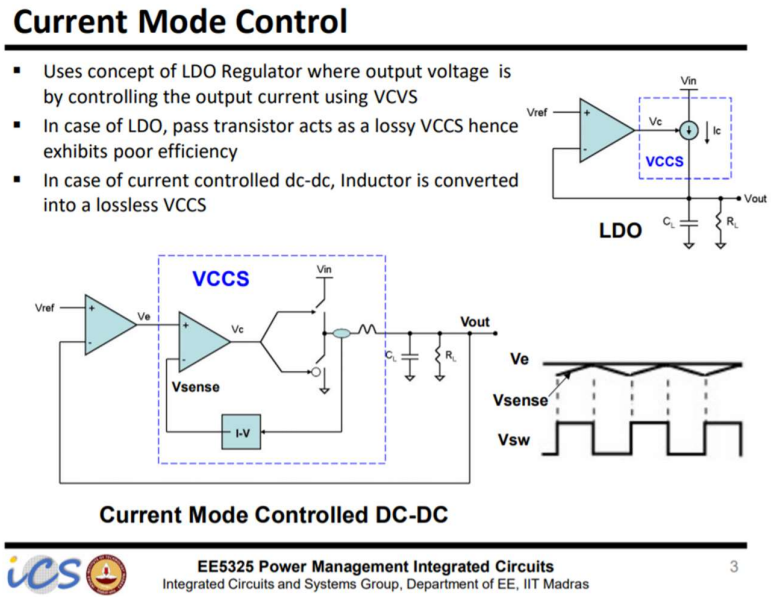


You can imagine that after V_C, you have the PWM modulator and everything. I just simplified it that V_C is controlling the switches through your PWM modulator and then gate driver.

But the main thing to notice is we have LC here, which causes complex poles, which makes the system inherently unstable. That's why we require complex PID compensation to achieve high bandwidth or good transient response. If you do not care about bandwidth, then you can use type-I compensation (just integral one) and push these complex poles outside ω_{ugb}, and you can get a simple compensated buck converter.

In Current mode control, we are sensing the inductor current and we have I-V converter, because we are having a control voltage not the control current. That's why you need to convert this current into voltage.

Now you can see there are two loops: one is the outer loop, other is the inner loop. Outer loop is comparing your output voltage with V_{ref}, which means it is regulating your output. And inner loop is regulating the current or limiting the current actually.

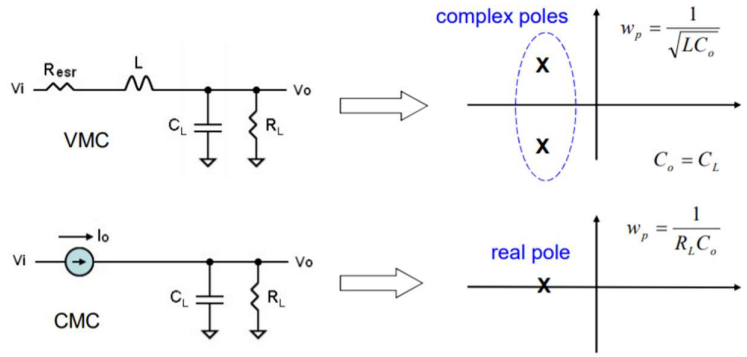


The sensed current is converted into voltage (V_{sense}). The moment your V_{sense} tries to cross your control voltage V_e, this V_c will go to zero and it will reset the duty cycle. This is basically nothing but your PWM modulator. But you do not have a ramp here because ramp is inherently coming from the sensed current. But instead of comparing V_e with any intermediate voltage, we are only using the peak information of V_{sense}. So, it limits the peak current.

If I keep limiting the peak current and I assume that my duty cycle remains constant, then this inductor average current will always be constant. Which means inductor average current is regulated. If it tries to go above or below this, this current loop will try to bring it back to the same point by changing the duty cycle. Which means, that resonance is killed by limiting the current and your inductor will behave like a voltage controlled current source (VCCS). If inductor is converted into VCCS, then you do not have any complex poles and the only pole will be at $s = \frac{-1}{R_L C_O}$.

Complex – Real Pole Transformation

- Unlike the Voltage Mode controlled, the complex poles due to L & C is converted into real pole because of the inner current loop

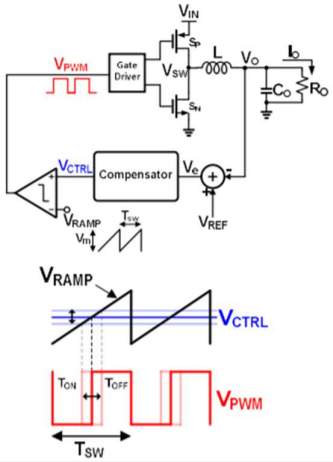


So, whatever bandwidth you can achieve with type-III in voltage mode control, you can achieve similar kind of bandwidth in current mode control by simply using type-II.

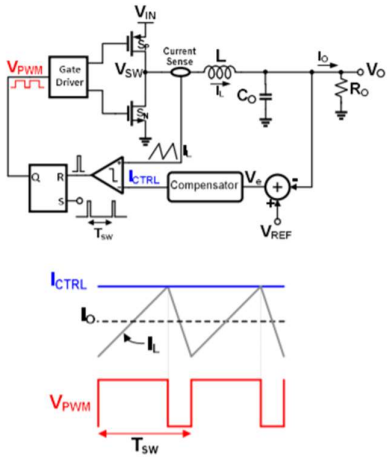
The voltage mode and current mode controllers are shown in below figure.

Voltage Mode Vs Current Control

- Duty cycle is controlled only by voltage
- Uses an external ramp



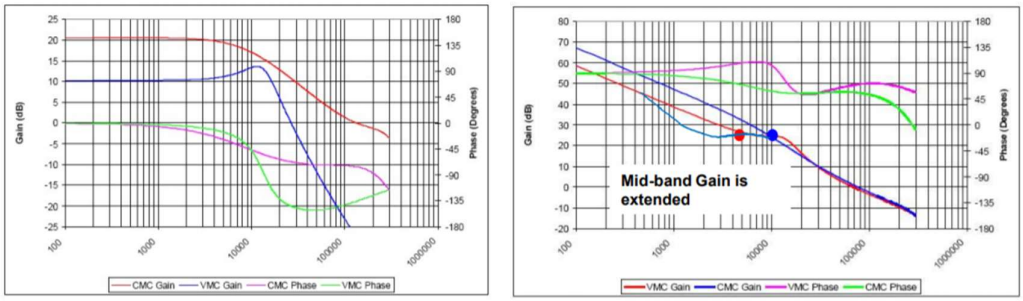
- Duty cycle is controlled by both voltage and current
- Doesn't require external ramp



VMC vs CMC Frequency Response:

In current mode control, phase and magnitude roll-off is not as steep as in voltage mode control. You will get smoother frequency response.

Brian Lynch, "Current mode vs. voltage mode control in synchronous buck converter", Texas Instruments



Before compensation

After compensation

With the uncompensated VMC gain, you will get a peaking due to resonance (left blue curve). But in CMC, I am limiting the current. So, I should not get any resonance and you will see a first order low pass filter kind of frequency response (left red curve). Similarly, the phase drop is steeper in case of voltage mode (left green curve). In current mode phase is not dropping that steeper (left pink curve). After compensation, frequency response is shown in right side figure.

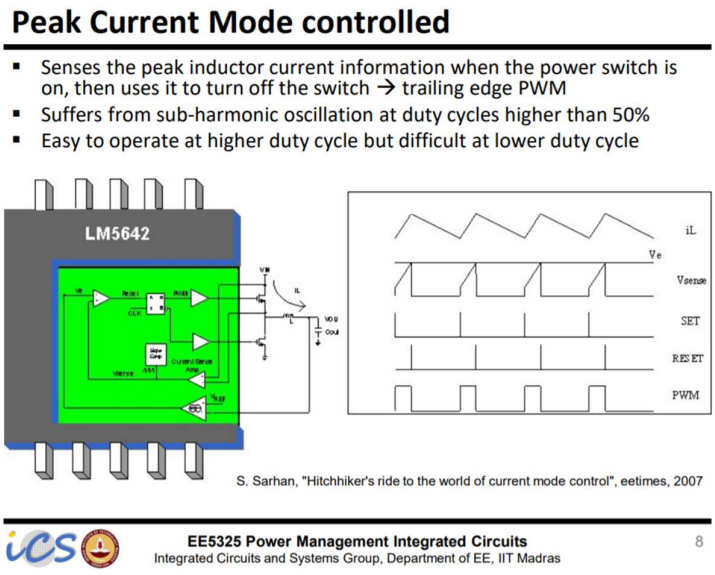
Current Mode Control Techniques

- **Peak Current Mode Control**
  - **Peak Current (high side) is used to control the duty cycle**
- **Valley Current Mode Control**
  - **Valley current (low side) is used to control the duty cycle**
- **Emulated Current Mode Control**
  - **Both peak and valley currents are used to control the duty cycle**

In peak current mode control, we limit the peak current. Limiting the peak current means you need to sense the peak current or high side FET current.

In valley current mode control, we limit the valley current. So, we need to sense the bottom FET current.

In the emulated current mode, both peak and valley current information is used to control the duty cycle. This is more like average current mode control because we have both peak and valley information, and from that you can calculate the average. But if you have only peak or valley, then you do not know what the average is.



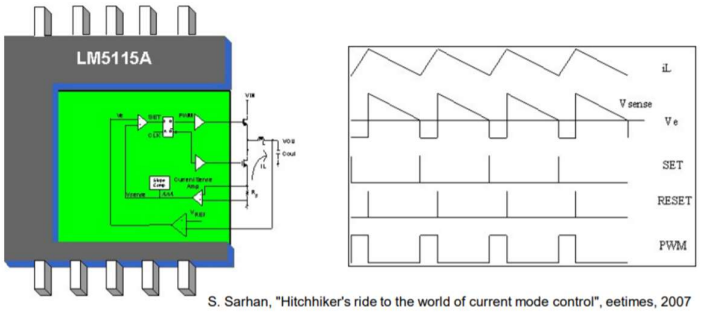
In the peak current mode, we are sensing only high side FET current. In the above circuit, high side FET is shown as NMOS but in our case it is a PMOS. But a lot of places we use NMOS at high side with the gate overdrive, because if your input supply is V_{in} then we can't apply V_{in} at the gate of high side NFET because it will drop one V_t. So, we use $V_{in} + V_t$ or higher voltage and that is done by using bootstrapping actually. There is a feedback capacitor which pumps this voltage up when this high side FET is turned on.

The reason we use NFET at high side is, because of higher mobility. So, your area will be much smaller or for the same area you will get a better $R_{ds,on}$. For high current applications, for high side FET also we mostly use NMOS.

Since we are sensing only high side FET current and we know that during the off time it will remain zero. When this high side current reaches control voltage (V_e), then the duty cycle will get reset. And your duty cycle is forced to set at your clock frequency. The waveforms are shown in above figure.

Valley Current Mode controlled

- Senses the valley inductor current information when the power switch is off, then uses it to turn on the switch → leading edge PWM
- Contrary to Peak CMC, it suffers from sub-harmonic oscillation at duty cycles lower than 50%
- Easy to operate at lower duty cycle but difficult at higher duty cycle

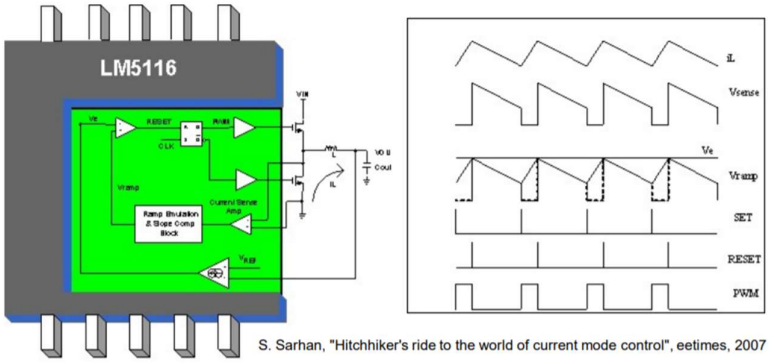


S. Sarhan, "Hitchhiker's ride to the world of current mode control", eetimes, 2007

In the valley current mode control, we are sensing only the bottom FET current. In this case, during off time you are sensing the current and we are setting the duty cycle at valley. Which means rising edge of PWM is going to move. So, you can say this is more like a leading edge. Your reset remains fixed at your clock frequency, but your set is determined by the valley current.

Emulated Current Mode controlled

- Uses valley current sensing to predict the peak current in order to emulate exact inductor current waveform
- Combines the advantages of valley CMC (low duty cycle operation) and peak CMC (good line transient)



S. Sarhan, "Hitchhiker's ride to the world of current mode control", eetimes, 2007

In emulated current mode control, we sense only the bottom FET current and we use it to predict the peak current in order to emulate exact inductor current waveform. So, in this case we can limit the peak as well as control the duty cycle by using the valley information.

Voltage Mode Control (VMC) vs. Current Mode Control (CMC)

Parameter	VMC	CMC
Line transient	Good with line feedforward ($V_M \alpha V_{IN}$)	Good (inherent line feedforward in peak current mode) Bad in valley CMC
Load transient	Good (bandwidth is independent of load current in CCM)	Good at high BW but degrades at lower load current (BW is dependent on load current)
Very low duty cycle operation	Good	Poor
Noise insensitivity	Good	Poor
Compensation	Complex (Type-III)	Simpler (Type-II)

Line transient: If you remember, in VMC we talked about line feed forward control, where your ramp amplitude (V_m) is controlled by V_{in}. So, it gives you better line transient.

In the case of peak current mode, so let's say V_{in} is increased. Then inductor rising current slope will increase and it will hit your control voltage (V_e) early and your duty cycle will reduce. So, inherently you have a feed forward control here. So, your line transient is very good compared to the voltage mode control.

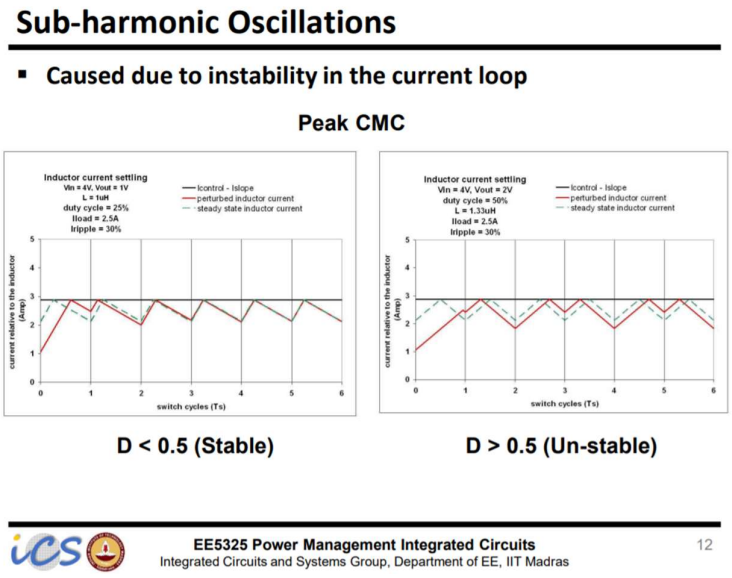
But if you use valley current mode then you would not get this advantage because slope of falling current is only depending on the output voltage. So, for good line transient we always use peak current mode control.

Load transient: In VMC, bandwidth is independent of load current. If you change the load current, bandwidth almost remains the same because your load only changes Q and your resonance frequency will remain same. Your zero locations will remain same and your gain will hardly change. So, your loop gain response and ω_{ugb} won't change. So, you will get good load transient response.

But in CMC, your pole is at $s = \frac{-1}{R_L C_O}$. If R_L is changing then your pole will change. So, your bandwidth is depending on your load current just like in the LDO, because your pole is moving.

Very low duty cycle operation: In VMC, very low duty cycle operation is good. But in CMC, it is poor because if you are operating at a very low duty cycle, then inductor current slope will be faster. So, during on time your current rises very fast and the current sense amplifier you require should be very high gain bandwidth. So, it will be limited by the bandwidth. So, you cannot sense very fast current and that will limit your low duty cycle operation.

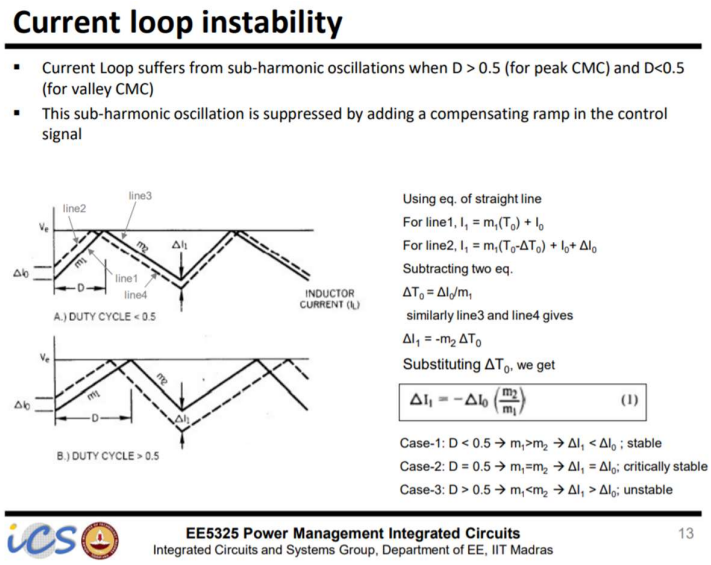
Noise insensitivity: Current mode control is more sensitive to noise because it will create sub-harmonic oscillations. Example for sub-harmonic oscillations for peak current mode control is shown in below figure.



Dashed one is steady-state inductor current and the solid one is perturbed which is disturbed. Let's say it is slightly shifted down. Since my control voltage, V_{in}, V_{out} and L are not changing; only inductor current is slightly disturbed due to some reason. Then slope of inductor current is also not changed because all the conditions remain same. So, it will take longer time to touch the peak and your on-time is stretched here. So, duty cycle is disturbed but all the conditions remain same. When you disturb the duty cycle, your output will try to change.

But the outer loop (voltage loop) is forcing V_{ctrl} to remain same. So, duty cycle is not changing. But the inner loop (current loop) is much faster because you are limiting the current in every cycle. Which means inner loop is very faster than the outer loop; almost 10 times or more than that. But your bandwidth is limited to one-tenth of your switching frequency. So, if control voltage is not changing then automatically this current loop will behave in such way, and it stretched out the on-time.

And for peak current mode control, set point for duty cycle remains same because it is synchronized to your external clock. Now your on-time has increased, and it gets lesser off-time. Ultimately the output loop should force it to settle. For D < 0.5, after few cycles inductor current was settled. But the problem is if D > 0.5 then it does not settle as shown in above figure.



To make ΔI_1 converge to 0, m_1 should be greater than m_2. Which means for peak current mode control, D should be less than 0.5 to avoid this instability. If D is greater than 0.5 then it will not converge, and you will get instability. And D equal to 0.5 is your critical condition.