Power Management Integrated Circuits
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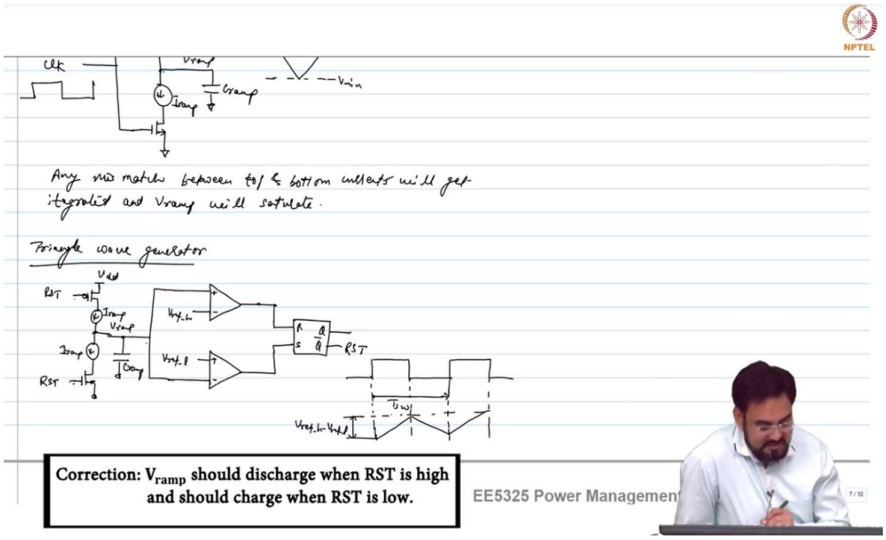
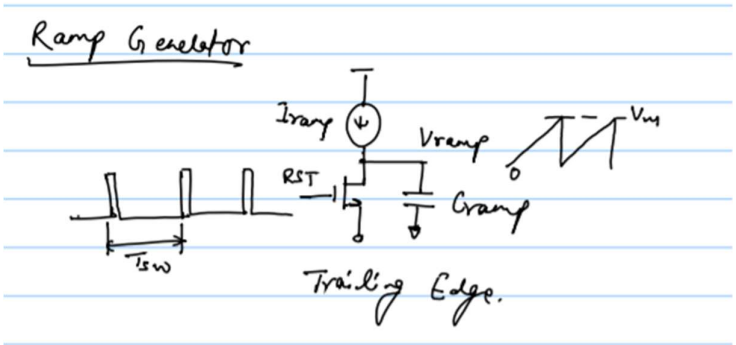
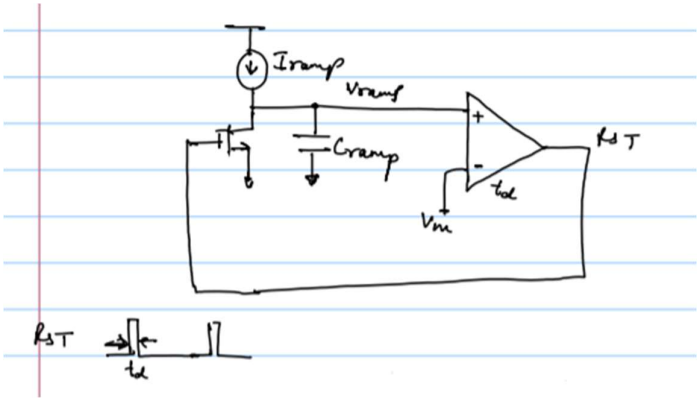
Lecture - 69
Average Ramp Voltage of Single-Edge PW Modulator, Design Considerations of EA

We can do dual edge modulator with the oscillator because it is not possible with the current sources alone.



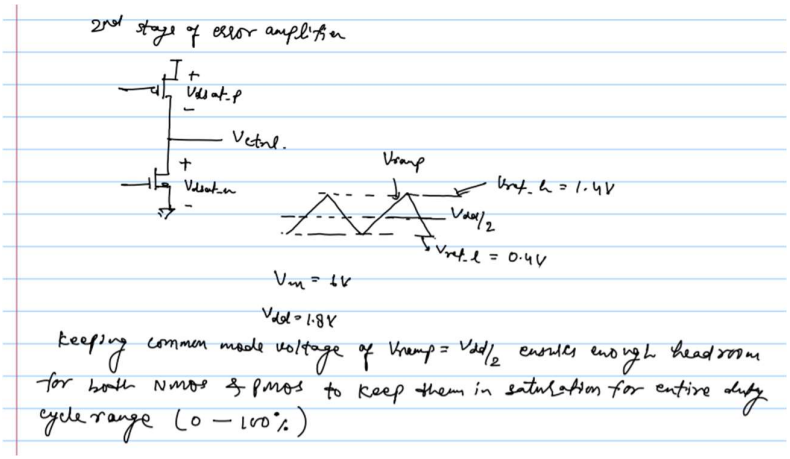
But single edge modulator is possible with the current source. And here we are limiting only one side voltage not two side voltage.





Whether you use an oscillator or simple ramp generator, how do we make sure that my common mode remains at $\frac{V_{dd}}{2}$? Because in both the circuits, we are resetting to 0. So, in trailing edge NMOS will reset V_{ramp} to 0 and in leading edge PMOS will set V_{ramp} to V_{dd}.

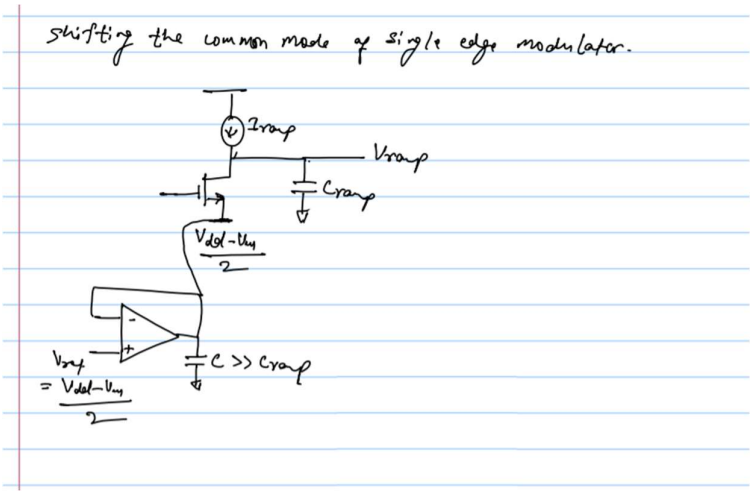
So, you are always starting from 0 or V_{dd} in this case. Your V_{ramp} is shifted towards V_{dd} or ground, common mode of V_{ramp} is not at the mid. So, this may have a problem. If you take trailing edge case, you can't operate at lower duty cycle. Let's say V_m is 1 V and the moment duty goes below 10% or so, then the control voltage will drop to 100 mV. At 100 mV, we cannot ensure that error amplifier's 2nd stage NMOS will remain in saturation, and my error amplifier gain will drop.



So, how do we fix this problem? You have to simply modify the existing circuit to shift the common mode.

Student: Replace the ground.

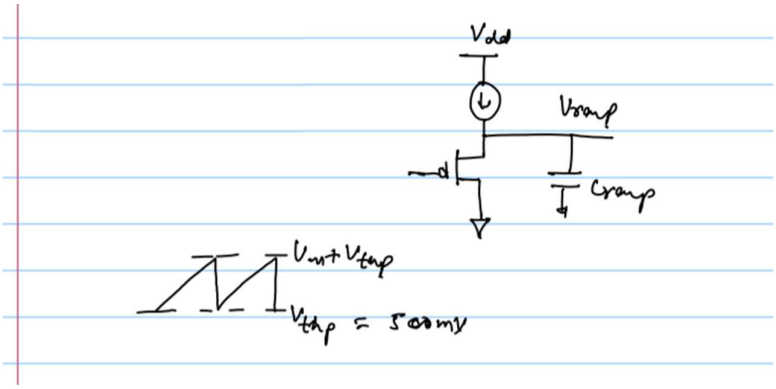
Yeah, you just replace the ground with another voltage so that it will always reset to that voltage. The modified circuit diagram is shown in below figure.



Let's say you replaced the ground with 0.4 V, and you kept everything else same. Now instead of 1 V it will charge to 1.4 V because you are starting from 0.4 V offset.

But at the output of buffer, you will require a huge cap because if this capacitor is large then only it can bring the voltage of the other cap to its level. If it is small, then it may not discharge, and it may remain much higher. Just a charge balance is happening; it has to draw all the charge from smaller cap, which means this capacitor should be large enough.

Can we use some other way; where I may not be very accurate but still, I can achieve the same kind of behavior? So, replace the NMOS with PMOS as shown in below figure.



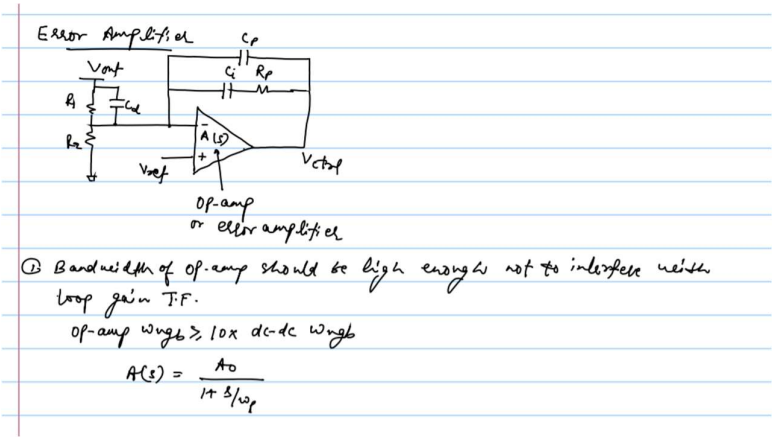
The minimum voltage PMOS can discharge to is $V_{th,p}$. This $V_{th,p}$ is roughly 500 mV and if you can use a little bit larger device then you can bring this $V_{th,p}$ close to 400 mV. So, these are the small things you need to take care when you are designing your DC-DC converter.

If your output voltage is always above 50% of V_{dd}, then you are always above 50% duty cycle. So, you do not care about the lower duty cycle because your control voltage will never go below $\frac{V_m}{2}$. In that case you can use NMOS with ground to reset your ramp to zero.

As long as your control voltage remains above 500 mV, output stage of your error amplifier will always be in saturation. If your operating at entire duty cycle range, then you have to shift the common mode of your ramp signal and you do not have any other option.

Error Amplifier design considerations:

1. Bandwidth of op-amp should be high enough not to interfere with loop gain transfer function.



We know that your compensation network is built around your error amplifier or op-amp. One thing you need to consider is bandwidth of op-amp should be high enough not to interfere with loop gain transfer function. We do not want additional pole from your op-amp because here we are introducing integrator with 2 zeros, and then on top of that we put 2 more high frequency poles due to noise reasons. One high frequency pole is coming from C_p and other pole can be introduced by adding a resistance in series with C_d.

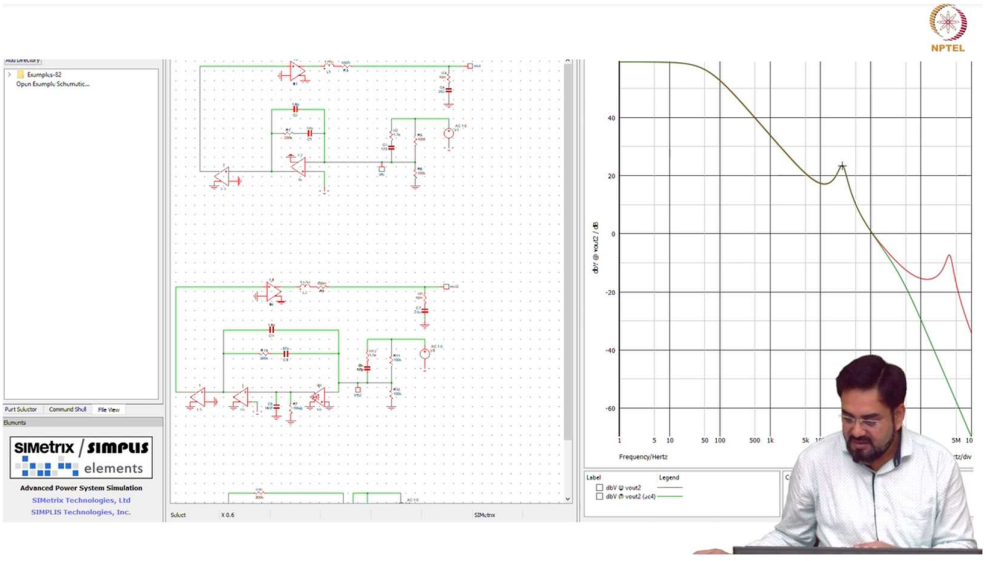
So, one more pole means, even if it is not inside ω_{ugb} but let's say it is at $5\omega_{ugb}$. Still you will get a significant drop in phase margin, maybe 5° to 10° which is significant. That's why we do not want the pole due to op-amp interfere with your loop gain transfer function. Most of the time we keep ω_{ugb} of op-amp greater than 10 times of DC- DC ω_{ugb}. The reason is this op-amp is not in the open loop, we have a closed loop network around that.

And if you model this op-amp with first order approximation then op-amp transfer function A(s) is given by

$$A(s) = \frac{A_o}{1+\frac{s}{\omega_p}}$$, where A_o is DC gain and ω_p is 3 dB frequency

So, ω_{ugb} of op-amp will be $A_o\omega_p$. Whenever you connect any op-amp in a feedback then you always look for ω_{ugb} because at high frequency capacitors C_i and C_p will be shorted and op-amp will act more like a unit gain amplifier. In that case until ω_{ugb} you see a flat response. So, in closed loop your 3 dB frequency is shifted to ω_{ugb} .

2. High frequency poles (outside ω_{ugb}) in type-III compensator help in suppressing the additional resonance which might occur due to the limited bandwidth of the op-amp or due to the internal poles of op-amp. The loop gain response without high frequency poles (red curve) and with high frequency poles (green curve) is shown in below, by modelling op-amp with first order approximation.



And if you replace op-amp with the second order, then this resonance may look even worse actually. You might think of moving these poles at much higher frequency or just get rid of these high frequency poles to get a better phase margin; because these high frequency poles will cause some drop in the phase margin, maybe 5° to 10°.

So, if you try to get rid of these poles just to increase the phase margin, then you have to be a bit careful because you may have that additional resonance and it may cause some kind of instability in your loop. It is ok to have 5° drop in phase margin because if you are looking for 60° phase margin then instead of 60° you are getting 55°. You may still be ok, but this additional resonance is not good. Or otherwise you make your op-amp bandwidth very high, so that additional resonance won't affect your loop stability. But it will come at the cost of power consumption because to design very high bandwidth op-amp you need to burn a lot of power in your op-amp.

But this problem will not occur if you are using g_mC compensator because in g_mC everything is open loop. So, we will not see any additional resonance in g_mC. Your design may become simpler with g_mC because this instability problem may not happen. So, if you can design your g_m in such a way that your offset is not that high then you may prefer to go with g_mC.

3. We are free to use any op-amp topologies: folded cascode or simple 2-stage or telescopic as long as you meet the performance.

If the gain requirement is 60 dB, then you may go with a simple 2-stage opamp. If your gain requirement is a bit lower, then you can go with single stage op-amp. If you want to increase the gain with a single stage op-amp, you can go with telescopic where you cascode in the single stage and get higher gain by increasing R_{out}.