Power Management Integrated Circuits
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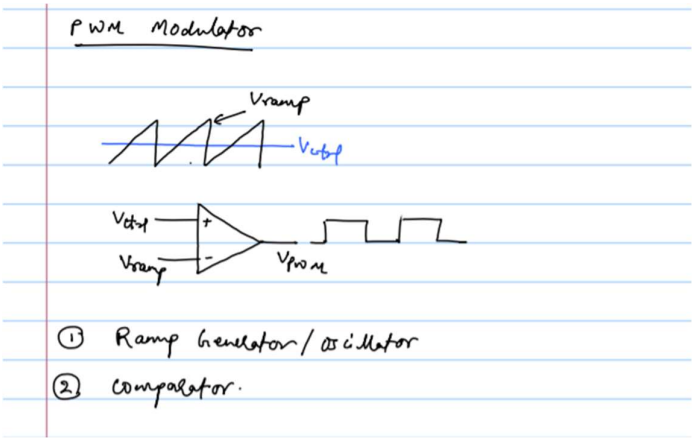
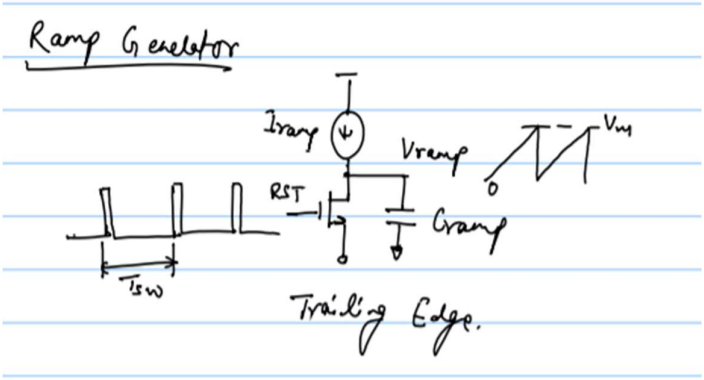
Lecture - 68
Pulse-Width Modulator: Trailing Edge, Leading Edge and Dual Edge; Triangle Wave Generator

PWM modulator takes your control voltage (V_{ctrl}) and compares with V_{ramp} to generate the PWM signal. So, you need ramp generator and comparator.



If you already have the clock, then you can generate ramp from that. If you do not have the clock, then you need oscillator. And you can design the oscillator itself to give you the ramp directly. The ramp generator (trailing edge) circuit is shown in below figure.



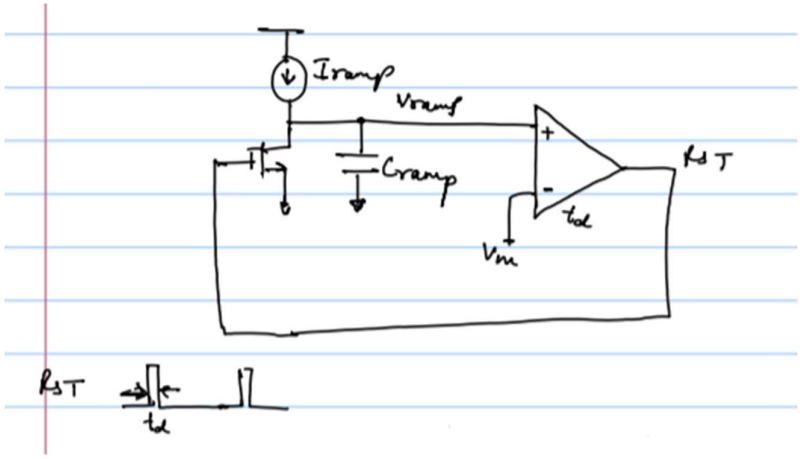
$$I_{ramp} = \frac{C_{ramp}\, V_m}{T_{sw}} \Rightarrow V_m = \frac{I_{ramp}\, T_{sw}}{C_{ramp}}$$

If C_{ramp} is smaller then you will require less current (I_{ramp}). But one thing you have to look into is, this V_{ramp} is going at the input of your comparator. So, while choosing C_{ramp}; make sure that whatever the parasitic capacitor you have at V_{ramp} node, that should be very small portion of your C_{ramp}. That's why we choose minimum 1 pF and based on that we choose the current.

Student: Sir, how we decide the switch size?

You have to make sure that this switch should be able to discharge to zero within the reset time. If your PWM signal is only controlled by this ramp, then this reset should be very small portion of T_{sw}. Let's say my switching frequency is 1 MHz which means T_{sw} is 1000 nanoseconds, then usually we keep this reset time order of 1 nanosecond so that it should not affect your PWM because we are looking at a single edge modulation.

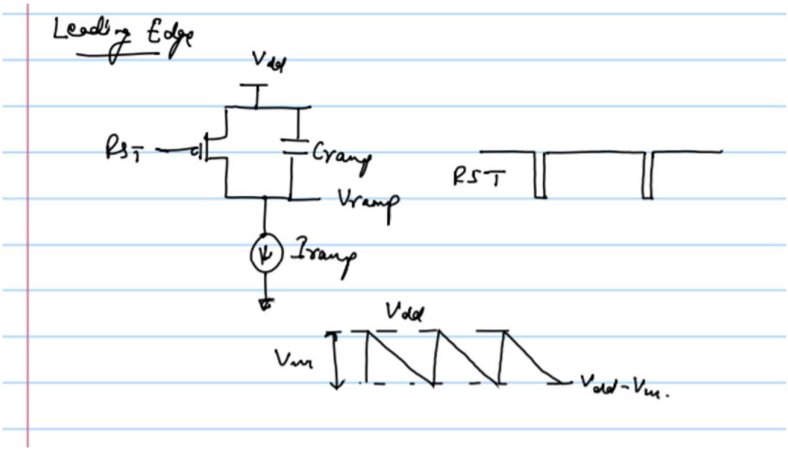
Let's say I am not given the clock, then we have to design the oscillator. And the circuit diagram is shown in below figure.



The moment V_{ramp} goes above V_m, this comparator will pull the gate high and it will reset. And as soon as it gets reset, the state of the comparator output will be low, and this switch will automatically turn off. So, your reset time will depend on the delay of this comparator. Which means if you keep your comparator delay as 1 or 2 nanoseconds, then that will become your reset time.

The advantage with this oscillator is, let us say if your current is changing then it will only affect your frequency but ramp amplitude (V_m) will always remain constant because you are comparing with the comparator.

Ramp generator (leading edge): the circuit diagram is shown in below figure.

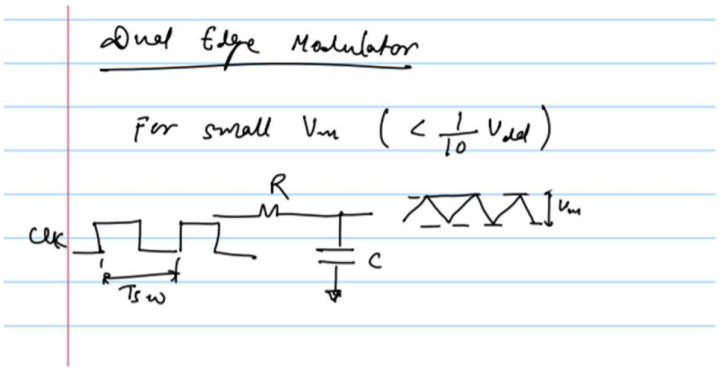


Use PMOS and set it and you will discharge as shown in above. And if you want to do the oscillator, you can do the same way but now your comparator will reset, and the waveform you get at the V_{ramp} will be exactly like this.

Now, how do we do the dual edge?

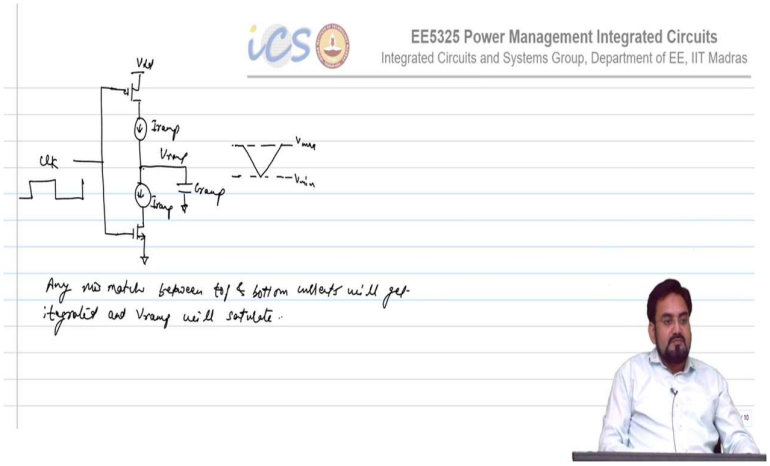
Student: Increase the comparator delay (t_d) to increase the reset time.

But your slew rate will depend on the MOSFET resistance. You are charging with the current and discharging with MOSFET resistance, so there will be a mismatch between the two. If you are charging with current, you want to discharge with the current. And now you are discharging through a resistor, so it will have exponential behavior and non-linearity will be there. For a small signal it is fine. I would say for V_m less than one-tenth of V_{dd}, you get a perfect triangular wave at the output as shown in below figure.



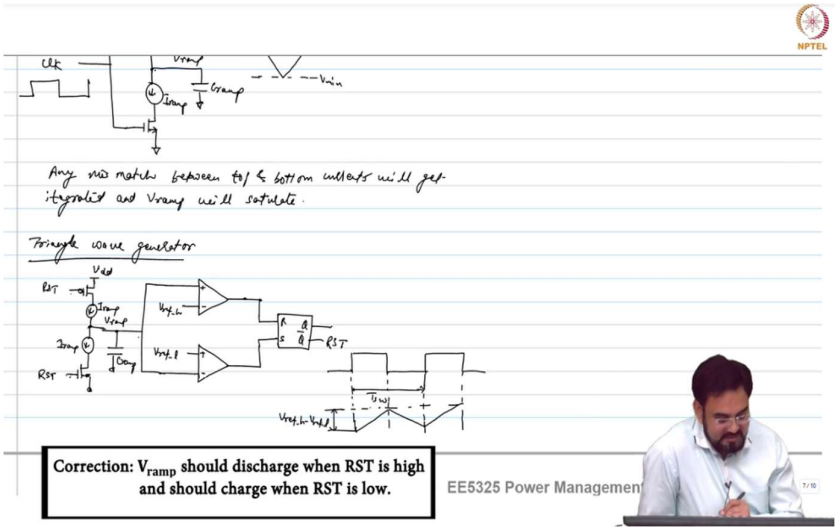
But the moment you start increasing the V_m, you will see exponential behavior and non-linearity will come into picture. And your loop gain will not have the same relationship. Now, the modulator gain $\frac{1}{V_m}$ will become something else.

So, you need both charging and discharging currents as shown in below figure.



But the problem with the above circuit is mismatch between the currents. Let's say Δi is the mismatch between the currents. So, Δi you are dumping into the capacitor or drawing out of the capacitor. So, you are integrating $\pm\Delta i$ and it will saturate to 0 or V_{dd} because capacitor is nothing but a current integrator.

So, any mismatch between these currents will get integrated and will saturate your output. To avoid this problem, limit both high and low voltages. So, output will never saturate. To achieve this, you need two comparators as shown in below figure.



You use $\overline{Q}$ as reset (RST) signal and it will be a square wave. So, $V_{ref,H}$ - $V_{ref,L}$ will be the peak-peak amplitude of triangular wave. And we will keep this difference equal to V_m .

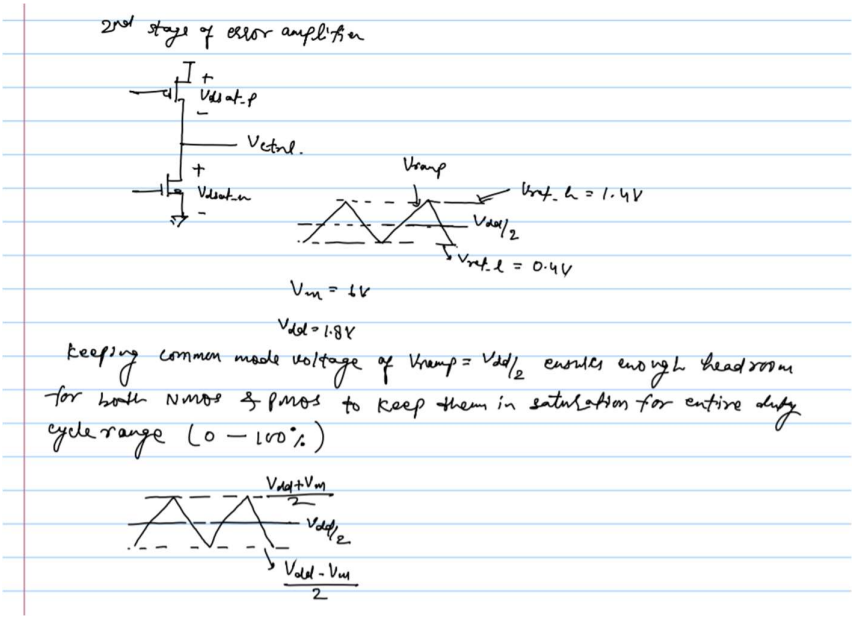
Now, how do we choose this $V_{ref,H}$ and $V_{ref,L}$?

Student: Whatever the range of control voltage.

How do you define range of control voltage?

Student: $\frac{V_{dd}}{2} \pm \Delta V$.

Yeah, your error amplifier output is nothing but your control voltage. Error amplifier's 2nd stage is shown in below figure.



Even when you are operating at a lowest duty cycle or max duty cycle (0% or 100%), you have to make sure that both the devices of error amplifier's 2nd stage are in deep saturation. Otherwise your DC gain will drop, and your UGB may drop. So, your loop gain behavior will change. You may even get a large output error if you are operating near 0% or 100% duty cycle.

So, keeping the common mode voltage of $\frac{V_{dd}}{2}$ ensures enough headroom for both PMOS and NMOS to keep them in saturation for entire duty cycle range.