Power Management Integrated Circuits
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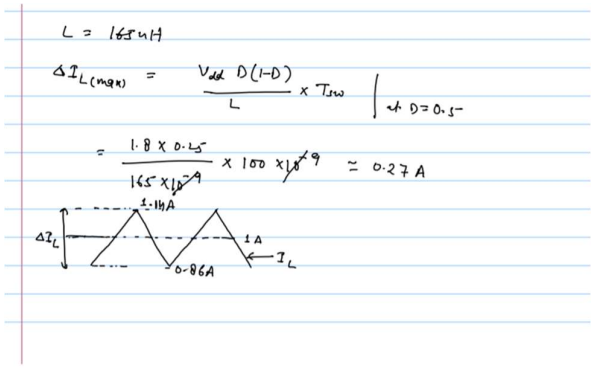
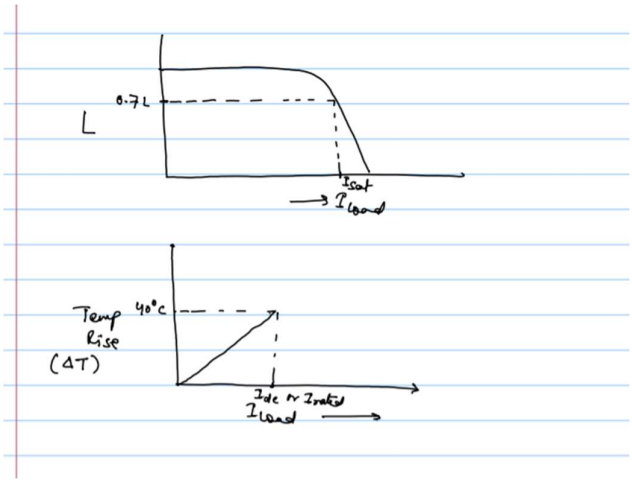
Lecture – 66
Inductor and Capacitor Characteristics, Reducing the Effect of Capacitor ESL

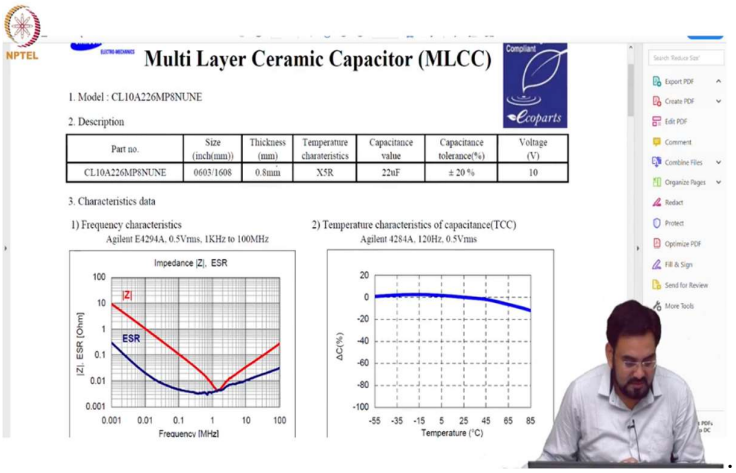


So, inductor should be able to support minimum peak current of 1.14 A. Inductor has two specifications. It has RMS current and saturation current. Sometimes they call RMS current as I_{rated} or I_{DC} and it is based on the temperature rise. Saturation current (I_{sat}) is based on inductor core saturation and that will be the worst case. When your inductor is saturated it is gone.



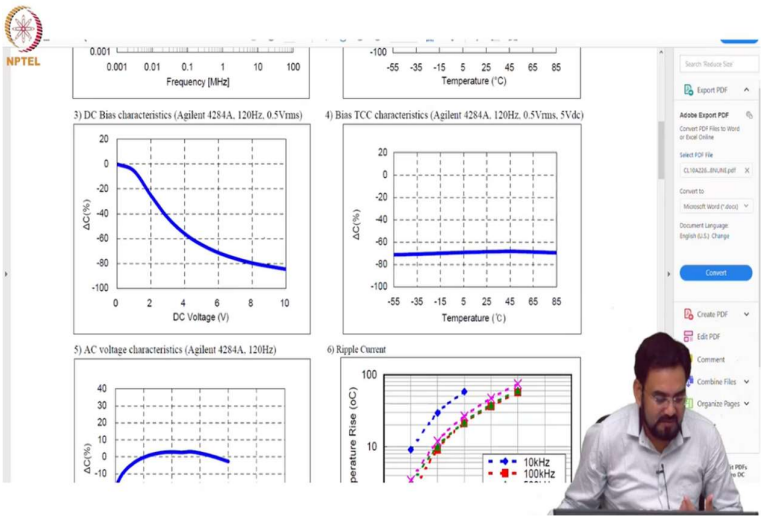
I_{sat} is the current at which your inductor value drops by 30% as shown in above figure inductance Vs. I_{load}, and then you have another curve temperature rise Vs. I_{load}. Temperature rise means extra temperature from whatever the temperature you are measuring at. For example, if you are measuring at room temperature then room temperature plus 40°C. If you are measuring at 100° C, then it should be 140°C.

So, first let's look at the capacitor datasheet. If capacitor has parasitic inductance, then resonance will happen. Just like equivalent series resistance (ESR), you have equivalent series inductance (ESL). So, it will have some resonance and at that resonance, capacitor impedance will be same as ESR as shown in below figure.



And you can see, this ESR is exactly overlapping with the bottom of your resonance. At higher frequency your impedance will be high because of the inductance. But if there is no inductance, then impedance will be limited by your ESR. So, impedance will flatten out, but ESR is also usually a function of frequency as shown in above figure.

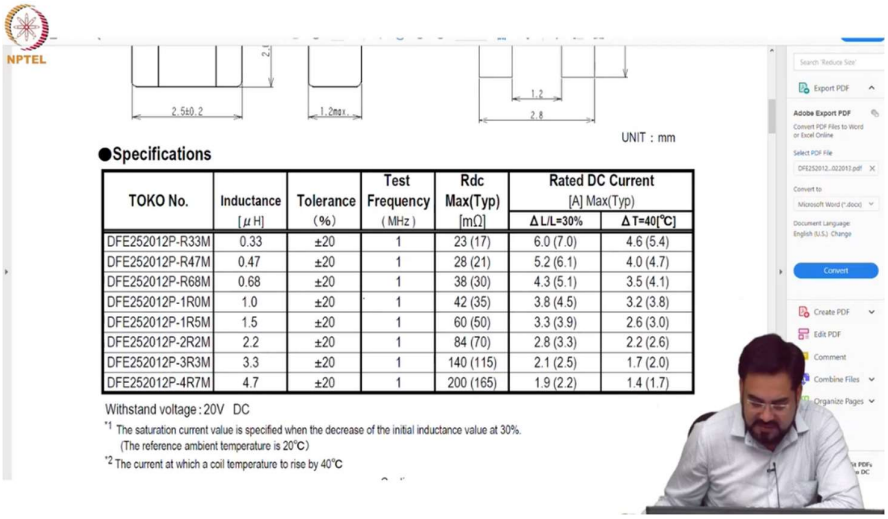
Temperature behavior is not that bad. You can see in above figure that temperature is not causing much change in capacitance; hardly 10% or so.



Now look at the characteristics with respect to DC voltage. Variation in capacitor is 0% at 0 V, and it drops below 20% at 2 V. Below 20% means you get 80% of the total cap value. And it drops by 80% at 8 V, and you will get 20% of total cap value. So, you have to be a bit careful when you are choosing the cap.

This cap rated voltage is 10 V and when you are very close to 8 V or beyond you may not get any cap. 10 µF will become like 1 or 2 µF and you will not meet your ripple spec in that case. Which means you have to put 4 or 5 caps in parallel. Usually you put in parallel, the reason is if you just take a single cap of 100 µF, then ESR and ESL will be high. But when you connect in parallel your ESR and ESL of all capacitors will be in parallel and they will get divided. So, you will get a better effective cap compared to the other case.

Now, let us look at the inductor datasheet. We have different values starting from 0.33 µH to 4.7 µH. The lower inductor has a lower DCR as shown in below table. Now think about DCR for 165 nH. It may be like 12 mΩ or so. And in our calculation, we considered DCR as 50 mΩ which is very high actually. It would not harm anything; in fact, your efficiency will look even better because your conduction losses will be much lower in the inductor compared to the DCR of 50 mΩ.



TOKO No.	Inductance [µH]	Tolerance (%)	Test Frequency (MHz)	Rdc Max(Typ) [mΩ]	Rated DC Current [A] Max(Typ) ΔL/L=30%	Rated DC Current [A] Max(Typ) ΔT=40[°C]
DFE252012P-R33M	0.33	±20	1	23 (17)	6.0 (7.0)	4.6 (5.4)
DFE252012P-R47M	0.47	±20	1	28 (21)	5.2 (6.1)	4.0 (4.7)
DFE252012P-R68M	0.68	±20	1	38 (30)	4.3 (5.1)	3.5 (4.1)
DFE252012P-1R0M	1.0	±20	1	42 (35)	3.8 (4.5)	3.2 (3.8)
DFE252012P-1R5M	1.5	±20	1	60 (50)	3.3 (3.9)	2.6 (3.0)
DFE252012P-2R2M	2.2	±20	1	84 (70)	2.8 (3.3)	2.2 (2.6)
DFE252012P-3R3M	3.3	±20	1	140 (115)	2.1 (2.5)	1.7 (2.0)
DFE252012P-4R7M	4.7	±20	1	200 (165)	1.9 (2.2)	1.4 (1.7)

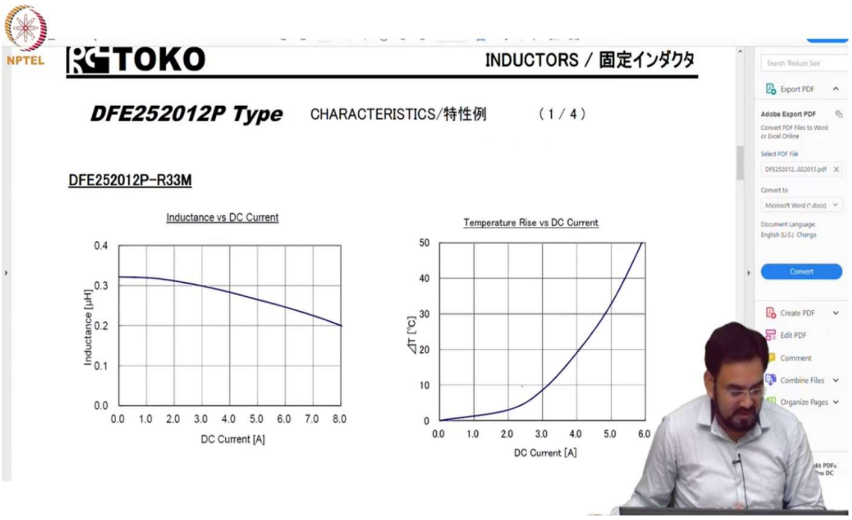
Under rated DC current column, you can see $\frac{\Delta L}{L}$ = 30%, which gives you saturation current (I_{sat}) and that is what we defined. You can also see that $\Delta T = 40°C$, which gives you I_{rated}. As inductor value goes lower, your I_{sat} improves and your I_{rated} also improves because I_{rated} is based on temperature rise. Temperature will increase only when I^2R losses are more. If DCR is high, then temperature rise will be more.

If you choose 4.7 µH, then supporting 1 A current will be like you are at the edge because I_{rated} is only 1.4 A. So, you have to be a bit careful when you are choosing the inductor. And in first column of the table, 252012 number says that 2.5 mm is the length, 2 mm is width and 1.2 mm is height. So, the package also depends.

Let's say you are looking for the same value of inductor in a smaller package then all the specs will change because smaller size means your thickness of the coil and everything will change and your DCR will increase. Let's say for 1 µH, I am looking at 10 mΩ kind of DCR then your inductor will be really big. And you can look at any converter which is catering to 10 A kind of current, you can find that inductor will be the biggest component there.

But for cell phone applications, we can't have that big inductor because it is mostly limited by the height because your phone thickness is limited, and your board size is also limited. If you open your phone you will see that the board will hardly occupy like 20 to 25% of the total real estate and battery almost occupies 40% kind of space.

So, you are left with very limited space and in that left-over space you have to place your speaker, you have to place your camera and everything actually. So, you cannot put a very big inductor there. Usually 2 mm x 2 mm and 2.5 mm x 2 mm package sizes we use for cell phone applications. And the biggest inductor you might see in the battery charger because that is where we charge with high current and especially fast charging and all those require very high current.



You can see in above figure that inductance value is dropping as you increase the current. This is for 0.33 μH and when it drops by 30%, which means the current at which you get 70% of 0.33 μH is your I_{sat}. And in other figure when temperature reaches 40°C, that gives you I_{rated}. The reason 40°C rise we choose is, most of these materials are defined to handle maximum temperature of 125°C or so. And if you take data sheet of any product, you will see the maximum ambient temperature they will define is 85°C or so.

85°C plus 40°C is nothing but 125°C. Beyond that we can't guarantee the operation and your inductor may even break actually. So, this temperature rise may be ok but in saturation there are two types. This is a soft saturation; you can see the curve shown in above is not that steeper.

And the hard saturation mostly happens if you have a magnetic core. If you have non-magnetic core, let us say air core or even metal core then you will see a soft saturation. And most of these smaller package inductors will have a soft saturation because they do not have a magnetic core. Magnetic core inductors are really big, and they are not feasible to implement in a smaller package and that's why if you look at any power inductor, you will find that this saturation curve is much steeper. For those kinds of inductors, you have to be a bit careful. You should have enough margin because the moment it hits your saturation your inductor value will drop quickly, and it will increase your peak current.

Let's say you have1 μH and it drops to 100 nH. So, 10 times increase in the peak current. It will break powerFET and everything. That is one of the reasons you require current limit, so that you can turn-off your powerFET immediately and you can protect your inductor.

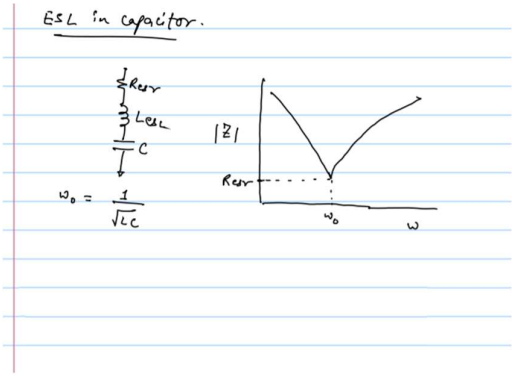
There is something called self-resonance in the inductance. Since these inductances will have parasitic caps and based on that parasitic caps, they will have a self-resonance. So, when you choose an inductor you have to make sure that self-resonance of this inductance is much higher than your switching frequency. Otherwise you would not get any value of the inductance, basically that inductance is dead because it is resonating. These were the things you need to consider while choosing inductor.

Student: Sir, usually after resonance only the inductor part starts dominating.

No, it is not like that. Inductance value will drop very quickly after resonance because parasitic capacitor will be in parallel with inductor and at high frequency it will short and you would not get any inductance value.

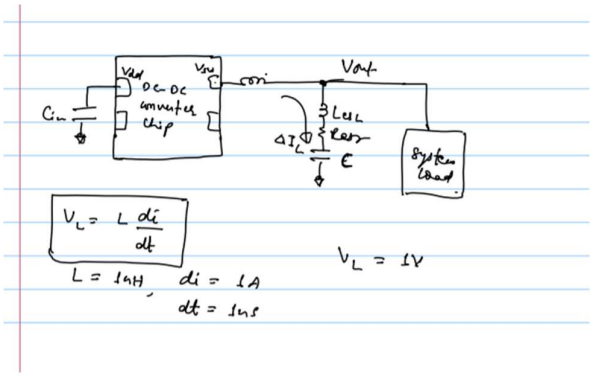
ESL in capacitor:

Capacitor model with R_{ESR} and L_{ESL} is shown in below figure. And the impedance graph is also shown.



You want your capacitor to behave as a capacitor. But if you look at beyond resonance frequency (ω_o), it is behaving like inductance and you do not want to. So, this ω_o should be much higher compared to your switching frequency otherwise your output ripple will be quite large.

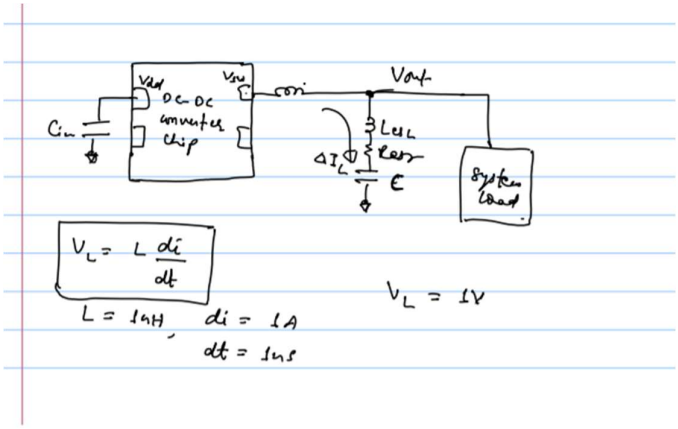
Other thing you need to take care of is while placing the cap. Let's consider your DC-DC converter chip. In below figure chip is shown only with few pads. And to the V_{sw} node LC filter is connected, and real model of capacitor is used.



When you are connecting your capacitor to inductor; from output to the capacitor when you are drawing the trace, you have to make sure that the trace length is minimized. Otherwise that will also add some inductance and it will be added with your L_{ESL}. And when you are connecting the cap, you have to make sure that this capacitor is closer to your system because you want to avoid the trace resistance also.

We know that the current profile at V_{dd} will be like a pulsating current, completely on-off. So, you need even more effective cap at V_{dd} because we have more discontinuity at V_{dd} side and the amount of switching current which is flowing into V_{dd} or outside V_{dd} is much larger. It will go from 0 to peak current of ($I_{load} + \frac{\Delta I_L}{2}$). In this case, you can't even afford to have a longer trace here when you are connecting the capacitor at V_{dd}.

C_{in} is connected at V_{dd} as shown in below. You have to put this decoupling cap (C_{in}) at the input, without this C_{in} it will not work. And all these switching currents will be supplied by this capacitor.



So, if you have a larger inductance, let us say 1 nH. So, we know that

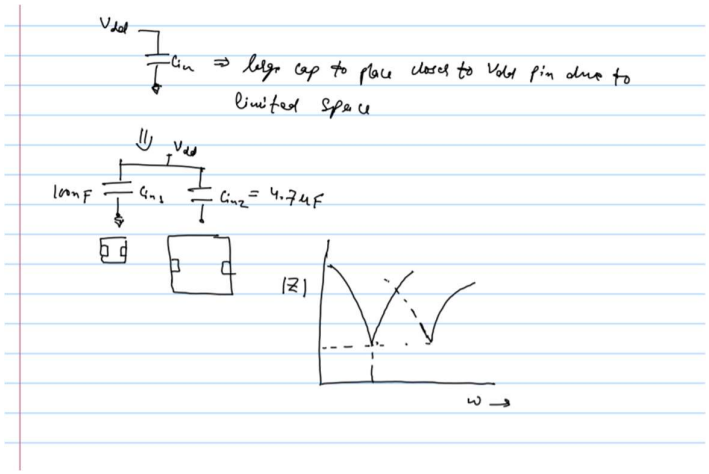
$$V_L = L \frac{di}{dt}$$

Let's say your di is 1 A. Since we know that we are rising very fast, so let's assume dt is 1 nanosecond. So, V_L will be 1 V. Which means it will cause a kind of a ringing because it will resonate. You are having V_{dd} of 1.8 V then on top of that you might see ±1 V undershoot and overshoot when it rings. Which will make it going from 2.8 V to 0.8 V. So, lower voltage may not be a problem from reliability point of view. In the worst case your system will not work.

But when you look at a higher side, it will cross the breakdown voltages of your devices and that may break. That's why this is very important when you are connecting the capacitor with a large $\frac{di}{dt}$. So, you have to make sure that your ESL is very small. Let's say I can afford may be ±100 mV or so, then the value of ESL you require is 100 pH.

But the parasitic inductance associated with this C_{in} will include the ESL of C_{in} itself. Whenever you are connecting this capacitor (C_{in}) to your V_{dd} node or any other pin, then that trace inductance will also add because that will be in series with L_{ESL}. That is one of the reasons, you connect more number of caps in parallel to minimize this L_{ESL}, rather than putting one single cap. But most of the time your chip size is not that big, and these pins are very closely packed. So, it is very difficult to keep the bigger cap as close as possible to the pin.

But if I have a smaller cap, then I can put that at V_{dd}. So, you use two capacitors in parallel (C_{in1} and C_{in2}). Let's say C_{in2} is 4.7 µF or so, then C_{in1} you can keep maybe like 100 nF. So, this C_{in1} can be easily placed closer to the V_{dd} pin compared to C_{in2}. So, you first place a smaller cap and then next to that you put a bigger cap. Now you will have two resonance.



Your impedance curve will look like as shown in above figure. And obviously the lower frequency resonance will be coming from the bigger cap. So, effectively at higher frequency, your impedance is not always increasing. This is more effective way of placing the cap if there is a risk of having larger ESL. Even this ESR will also come in parallel and that will also get reduced. So, it will benefit you in both the ways, in ESL as well as ESR.

This is how most of the time we do when we are placing the capacitor around your chip at a system level. So, this is very important. If you do not care about this, then there is a risk that your device may break because your 1.8 V devices can't tolerate 2.8 V. It will damage right away.

And we can't slow down the edges. I mean one way is like you just slow down the $\frac{di}{dt}$ by increasing the rise and fall time of those currents. By doing that you will be degrading the efficiency and limiting your duty cycle also. Because if your rise and fall time is more, then that will limit your duty cycle and your switching losses may also increase because if you remember the triangular one that will stretch (hard switching losses). So, we want switches to turn on as fast as possible.

This is the V_{dd} case and other one is the ground because bottom FET is also turning on. So, you care about that inductance as well. So, you have to make sure that it should not have inductance while routing the bottom FET and connecting to ground. Because series inductance in that FET, that will be looking like in series with the source of your bottom FET. Then at the source of bottom FET, you will again see this $L\frac{di}{dt}$ noise and that may again damage this FET.