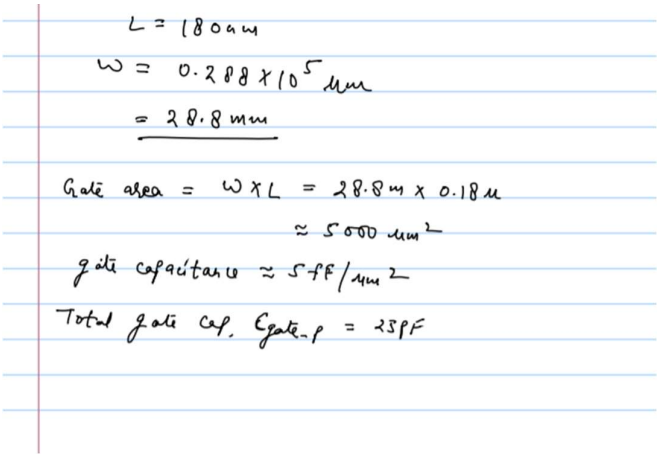
Power Management Integrated Circuits
Dr. Qadeer Ahmad Khan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture – 63
Estimating Switching Losses and Choosing the Switching Frequency

28.8 mm was the width we calculated for $R_{ds,on}$ of 70 mΩ. From this we can calculate the gate area and then we can find the gate cap as shown in below.



So, this gate capacitor for PMOS (C_{gate-p}) equal to 25 pF. So, for PMOS μC_{ox} is 70 $\frac{\mu A}{V^2}$. Anybody remembers the μC_{ox} for NMOS?

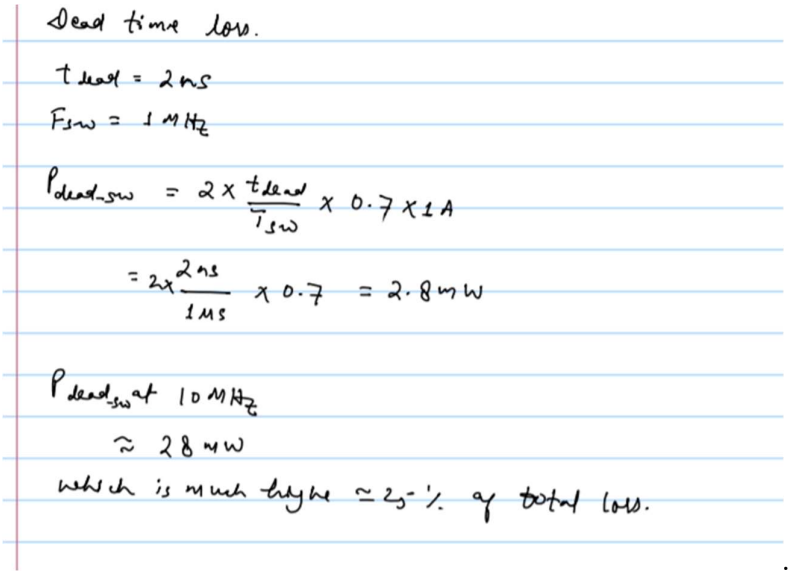
Student: 350 $\frac{\mu A}{V^2}$.

So, 5 times. Which means for the same $R_{ds,on}$, the NMOS device size will be 5 times less. So, C_{gate-n} will be 5 pF. So, total gate cap is 30 pF. Assume 1 MHz switching frequency. Switching losses is given by

$$P_{loss-sw} = C\ V^2 F_{sw} = 30 \text{ x } 10^{-12} \text{ x } 1.8^2 \text{ x } 10^6 = 100\ \mu W$$

Gate driver switching loss is approximately 100 µW. So, we still have a lot of margin, which means we can even operate at 10 MHz or so. If you operate at 10 MHz, you will loss 1mW and 1 mW is still a very small fraction of your total loss. This is ok for gate driver switching loss, but we have one more switching loss (dead-time loss).

At 10 MHz, if this dead time loss becomes very high then it will kill your efficiency. Then, we may have to go back and see the total switching losses at 1 MHz and 10 MHz. And then we will finally decide the switching frequency. So, let's find the dead time loss. Usually you keep 1 to 2 nano seconds kind of dead time.



So, at 1 MHz switching frequency dead time switching loss ($P_{dead-sw}$) is 2.8 mW. If you keep the same dead time at 10 MHz, that will be 28 mW which is very high. So, this will limit your switching frequency, or you reduce the dead time proportionally.

For 10 MHz, if you do not get dead time less than 2 nano seconds (like order of 100s of picosecond), then it will be very difficult to achieve more than 90% efficiency. Which means if you are running at a very high frequency, then it is not easy to achieve more than 90% efficiency even if your devices are very fast. That's why a lot of high frequency converters are designed for low current. Let's say your target current is 200 or 300 mA kind of number, then this switching loss will automatically reduce. But when you target amperes of current, it is not easy to run your converter at 10 MHz.

So, $P_{dead-sw}$ at 10 MHz will be 28 mW, which is much higher. At 10 MHz, efficiency will be

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{1200m}{1200m + 120m + 1m + 28m} = 88.9\ \%$$

So, instead of 90% efficiency you will get 89%. If you are happy with that, then you can go for 10 MHz, otherwise use a lower switching frequency.

But remember, you have to make sure that throughout the load current you have to maintain that efficiency as flat as possible. So, you have to make sure that your switching losses are not that high at light load. Let's say at 100 mW output power; you lose 25 mW in switching losses, then your efficiency will be like 70 or 75% which is very bad.

So, when you are operating at 100 mW kind of output power, then to maintain 90% efficiency your total loss budget is roughly 10 mW. I^2R loss will automatically scale down, but your switching losses will start dominating and this will limit your efficiency. So, you have to do some exercise; it is not like you choose at one load and just straight away decide the switching frequency and start designing. You have to make sure that throughout the load current, high efficiency is maintained and that is how you choose the switching frequency.

So, at 100 mA load current, output power is 120 mW. To get 90% efficiency total loss should be 13 mW.

$$P_{loss} = P_{out} \text{ x } \left(\frac{1}{\eta} - 1\right) = 1.2 \text{ x } 0.1 \text{ x } \left(\frac{1}{0.9} - 1\right) = 13 \text{ mW}$$

At 100 mA, conduction loss is 1.2 mW. ($\because R_{loss} = 120\ m\Omega$)

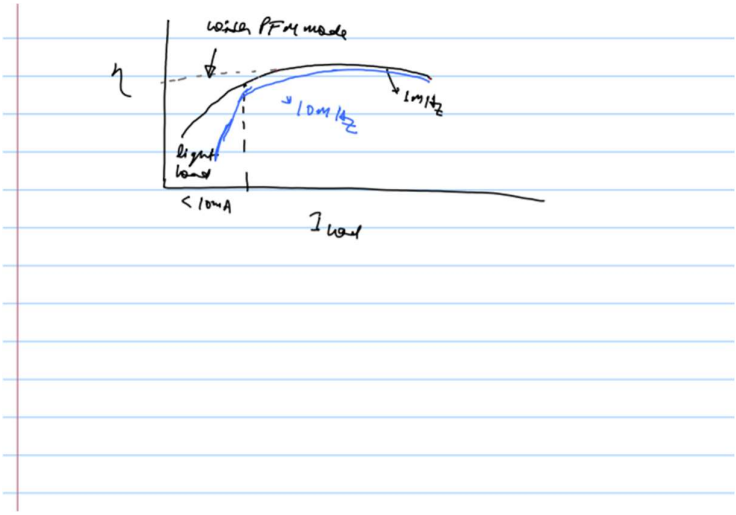
And your CV^2f losses will remain same. (0.1 mW at 1 MHz)

And your dead time loss at 1 MHz is 2.8 mW.

So, total loss is roughly 4 mW which is within 10% of total loss.

Which means at 100 mA also you will get 90% efficiency. Now, if you further reduce the load current let's say 1 mA, then it will start having problem. But usually at 1 mA or 10 mA you will enter PFM mode actually. So, you will start reducing the switching frequency at light load and you will maintain the efficiency curve as flat.

The efficiency curve with respect to I_{load} is shown in below.



Once you have a PFM mode you will maintain very high efficiency even at light load because you will start reducing the switching frequency. But if you do not have PFM mode then you will get very bad efficiency at light load. For 180nm process and for 1 A current; it looks like 10 MHz is not a big problem, you can easily operate and achieve high efficiency.

But instead of 1.8 V and 0.18-micron process, if you go to a 5 V process; 5 V process means those devices will have a high channel length may be like 0.5-micron kind of. So, roughly three times more than 0.18-micron process. So, your gate cap will also be 3x in 5 V process and your switching losses will be 3 to 4 times more.

We know that lithium-ion battery voltage is like 2.5 V to pretty close to 5 V. So, for the DC-DC converters which are operated at lithium-ion battery like mostly used in cell phones; this 1.8 V devices (180nm process) does not work and you need 5 V devices. With these 5 V devices, operating at 10 MHz is not easy if you want to cater 1 A current. You may achieve like 85% efficiency or so, but 90% efficiency is very difficult to achieve.

That's why so far if you look at any product in the market, the targeted current is like 800 mA or so, or less than that. So, 500 to 800 mA and maximum switching frequency of 6 to 7 MHz not more than that, and 10 MHz is very rare. But for this case, 0.18-micron and 1.8 V input voltage; 10 MHz switching frequency you can easily achieve.