**Power Management Integrated Circuits**
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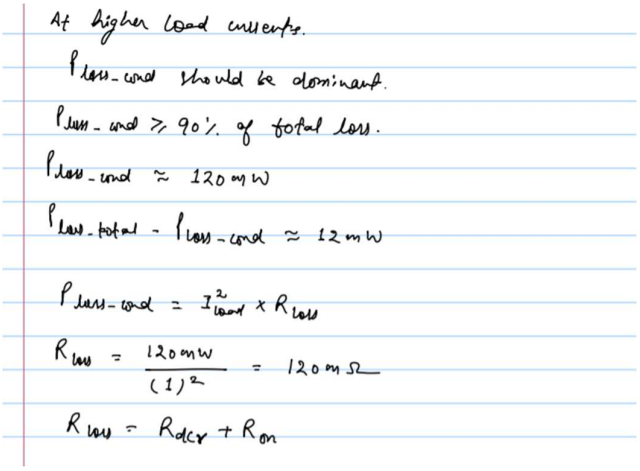
**Lecture – 62**
**Sizing Power MOSFETs**

At higher load currents conduction loss ($P_{loss-cond}$) should be dominant.




Now you have two choices, either you reduce $R_{on}$ and choose a bigger $R_{DCR}$ or other way around. Let's say out of 120 mΩ, I will keep $R_{on}$ as 20 mΩ and $R_{DCR}$ as 100 mΩ. So, 20 mΩ means your FET size should be big. So, we are losing area. And the switching losses, gate driver switching loss are also higher because the gate cap size will also be larger.

So, first you try to find the inductor with the smallest DCR. But let's say $R_{DCR}$ is not available below 50 mΩ, then you do not have any choice. So, I am just choosing a number, let us say $R_{DCR}$ equal to 50 mΩ which is quite realistic number and you can find a lot of inductors with 50 mΩ $R_{DCR}$. But when I say I want to have an inductor of microhenry ranges like 1 to 3 μH with 10 or 20 mΩ, then it may be difficult.

But for 0.47 μH, $R_{DCR}$ of 20 or 25 mΩ is quite possible. I mean for 1 μH, you can find 50 mΩ $R_{DCR}$ and now you are using half of that. So, the number of turns will also go half, and your coil resistance has to reduce. So, lower the inductor value smaller the resistance will be; if you are using the same material and everything remains same.

You will find the inductors in different packages. let us say you can find a 1 µH inductor in 2 mm x 2 mm package. And you can find the same value of inductor in 1 cm x 1 cm package also because it all depends on the thickness of coil. When you go for power inductors; it is supposed to carry 10s of amp and those inductors will be really big actually. I mean that maybe the biggest component on your board.

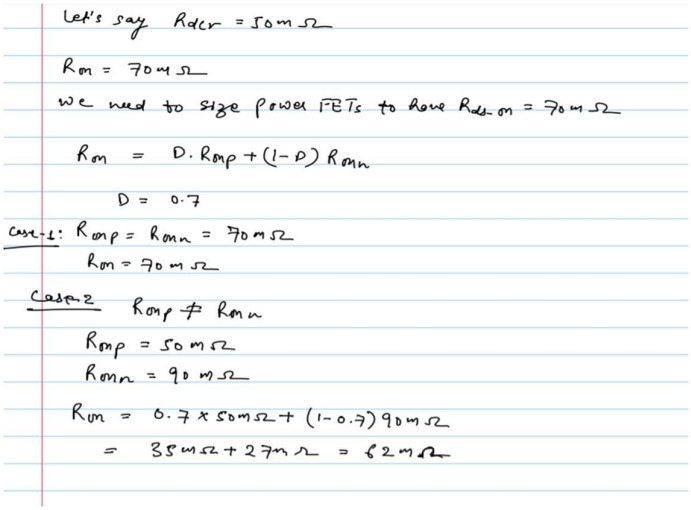
But when you talk about 1 A kind of a current, then you can easily find in 2 mm x 2 mm or 2 mm x 1 mm kind of package. The size will be quite comparable to your capacitor; like 10s of microfarad kind of capacitor.

So, now $R_{on}$ is 70 mΩ. But so far, we have not calculated the losses because in order to know the gate driver switching loss, first you have to size your powerFET to have $R_{on}$ of 70 mΩ. Unless you size it, you can never find $CV^2f$ loss, because C should be known.

Let us say I am keeping the size of PMOS and NMOS same and I know the mobility of PMOS is less; may be 3 to 4 times less. So, $R_{ds,on}$ of PMOS will be 3 to 4 times of NMOS. If your duty cycle is more than 50%, then high side FET or PMOS is conducting for longer time compared to NMOS. If you know the duty cycle range, then you can optimize this $R_{on}$.

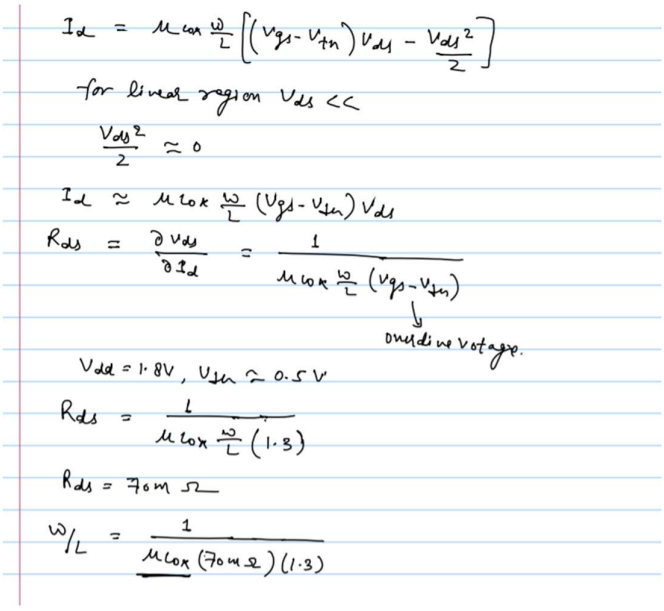
$$R_{on} = D\, R_{on,p} + (1\text{-}D)\, R_{on,n}$$

But if your duty cycle range is all the way from 10% to 90%, then you have to keep roughly the same $R_{ds,on}$ for both FETs, then you do not have any choice. But if you are always operating more than 50% duty cycle, then you can choose your PMOS bigger compared to NMOS, because you want to optimize the total $R_{ds,on}$. The example for D = 0.7 is shown below.



So, this is the one way you can try to optimize. But instead of D = 0.7, if I am operating at D = 0.3 or 0.4, then I would like to keep $R_{ds,on}$ of NMOS smaller than PMOS. While doing this optimization, you are keeping the area roughly same but total $R_{ds,on}$ is reducing because of the duty cycle. So, you can do these optimizations in the design.

For now, I will just go with $R_{ds,on}$ of PMOS and NMOS is same and equal to 70 mΩ. So, the first thing we need to know is the FET size. The formula for $R_{ds,on}$ of MOSFET when it is in triode region is derived below.




Since $R_{ds,on}$ is very low, so the IR drop will be very less. In the PMOS, $V_{gs}$ you are looking on the source side because the drain side potential will be slightly smaller because of this IR drop. So, always look for the higher side $V_{gs}$. But these standard CMOS devices are symmetric. So, it does not matter which side you are considering as source or drain, it only depends on the potential you are applying.

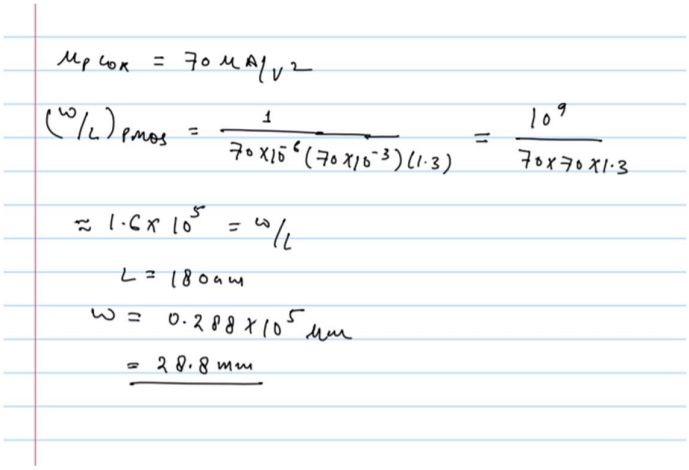
For PMOS and NMOS, $\mu C_{ox}$ value is different. So, for PMOS what is $\mu C_{ox}$?

Student: For PMOS it was 70 $\mu A/V^2$.

Is it simulated?

Student: In the process sheet it says.

Process sheet says, ok let us assume that. So, to get $R_{ds,on}$ of 70 mΩ, the width of the transistor required is 28.8 mm and the calculation is shown in below.




So, your width is 2.8 cm for minimum channel length (L). We use minimum length for these powerFET because we don't want to bloat the area.

How do you place this big transistor in your chip?

Student: Fingers.

Yeah, you split it into fingers actually. You can't choose a single finger, otherwise transistor will be looking like a stick. So, you connect smaller width transistors in parallel. Let's say you choose 100 µm as 1 unit. So, your total number of fingers will be 28.8 mm divided by 100 µm and that many fingers you have to connect in parallel. This is how you do in the layout actually, for big transistors.