Power Management Integrated Circuits
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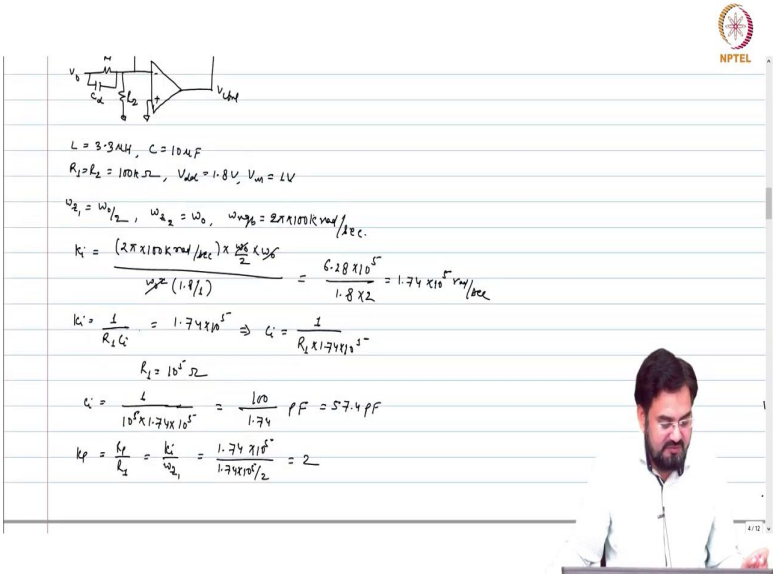
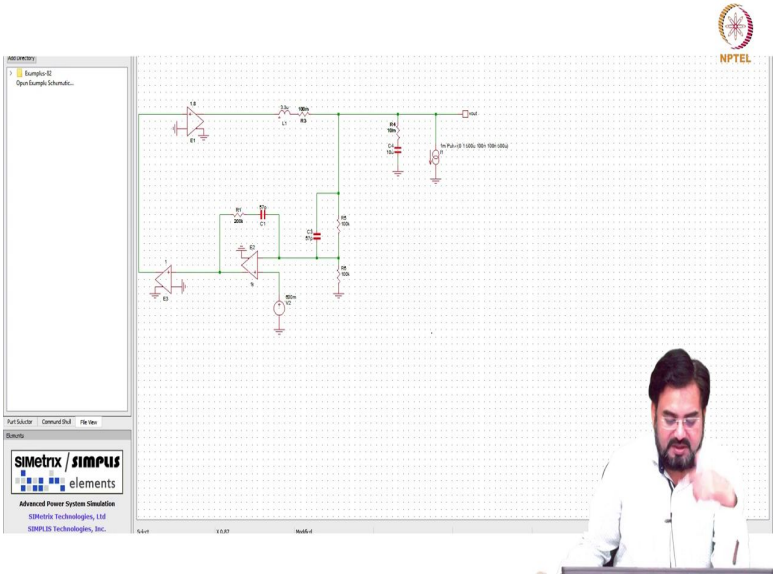
Lecture - 58
Simulation of DC-DC Converter with Type-III Compensator (Using Op Amp-RC Architecture)

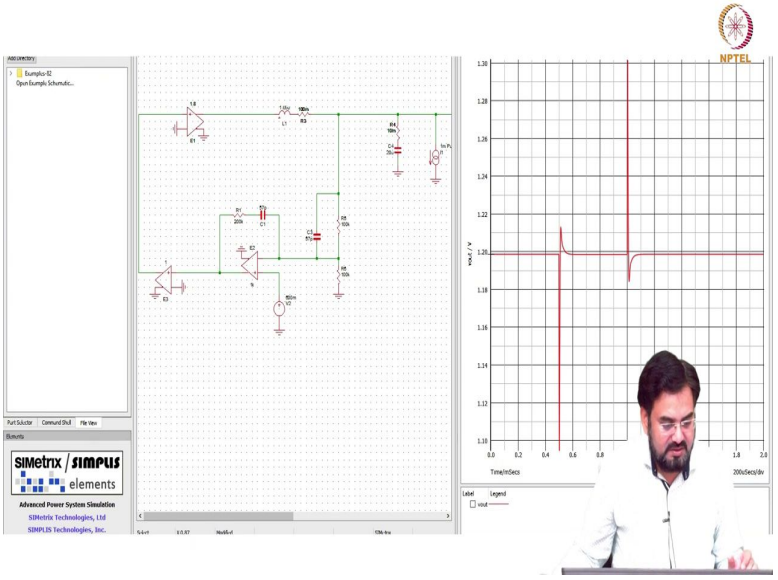


So, now if we change the values of ω_{z1} or ω_{z2} then values of components will change, but ugb should remain 100kHz. So, I have created one excel sheet, all you need to do in the excel sheet, just feed k_i formula and in separate columns have values of L, C, R_1, R_2, Vdd, V_m. So, all these values which I have put here you can have that. And whenever you are given the specification, you will be given the switching frequency; then from there you can calculate ω_{ugb} or it is quite possible that in the specification, you are only given input and output and you have to decide your L, C, switching frequency, etc.

But before you start the design, these values should be known whether it is given or not given. If it is not given then you have to find out what values of LC you want to choose, what switching frequency you want to choose based on efficiency and your ripple spec, and all those will be given. So, based on ripple spec also you choose values of L and C.



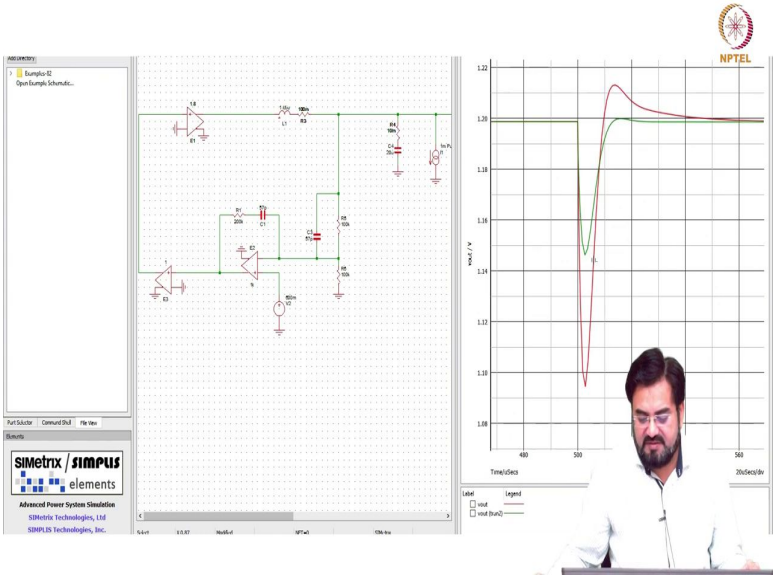
I am giving a switching load here. So, the output should settle. You will see undershoot and overshoot based on whether your load is getting removed or applied.



V_{ref} 0.6V and beta is half. So, you should get close to 1.2 volts and this error you are getting because I am putting a 60 dB gain here. So, your DC output will have some error and that error is only 2 millivolt or less than 2 millivolts or so. If I increase the gain, then it will go closer to 1.2V. So, you get a little as you see here peaking and then undershoot. So, this is mostly coming because of peaking in the magnitude response. If you reduce that peaking, then you can get a better response. You can reduce that peaking by reducing the Q.

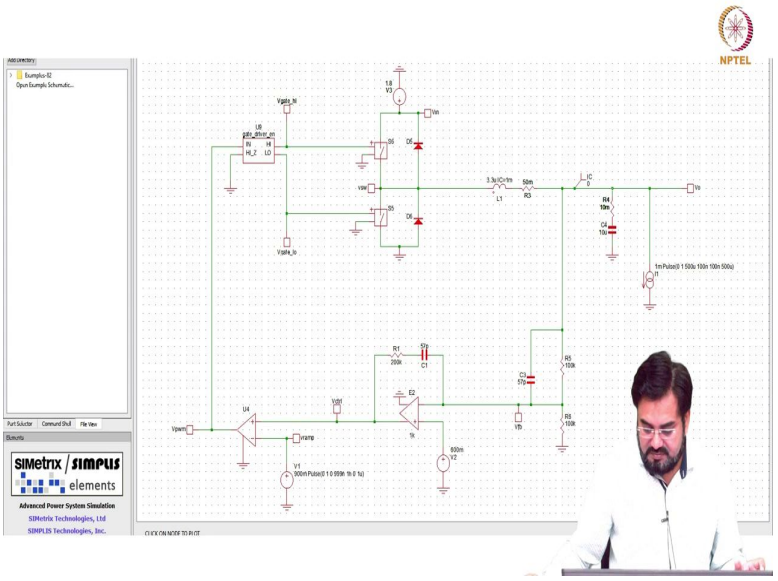
So, in order to reduce the Q, what we need to do? One way is to increase R_{loss}. But increasing the R_{loss} will kill efficiency. So, as another factor you had a square root L over C, and if I want to keep my resonance frequency the same because we have already calculated the values. I do not want to change my compensator. So, let us see you have already designed your chip for a particular ω_0, then you do not have an option to change then, but LC is external you can play with that.

We can make the inductor half and capacitor double. So, the product of L and C will remain the same. So, I will run it and plot on top of this and. So, one benefit you should get that your Q is reduced. So, this peaking should go away or at least should reduce, and another benefit you are going to get is that transient response improves because the slew rate is higher at a lower inductor value.

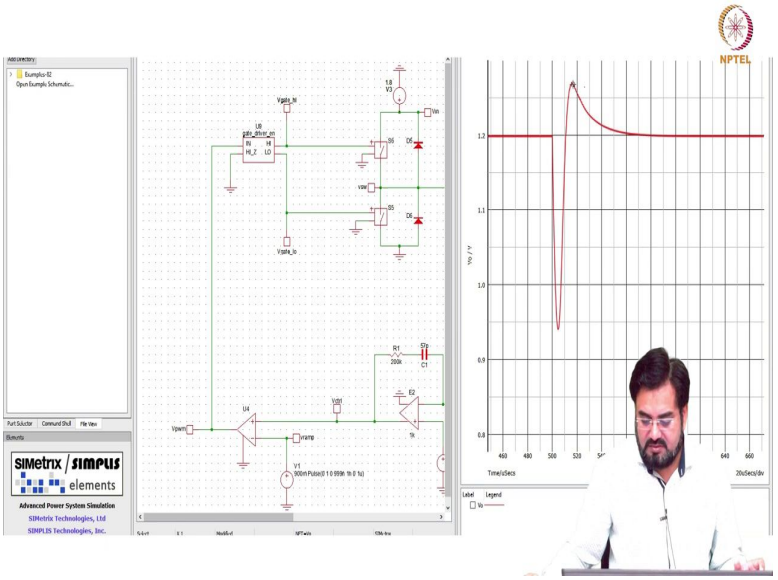


We will get huge benefits in transient response, simply by changing L and C. So, we already know that you have a square effect because your slew rate is getting faster because of the inductor and you are adding more cap. So, it will not discharge that much. So, that is why just by simply changing the L and C values, it is reduced by more than half, and your overshoot which you are getting due to that resonance peaking almost goes away.

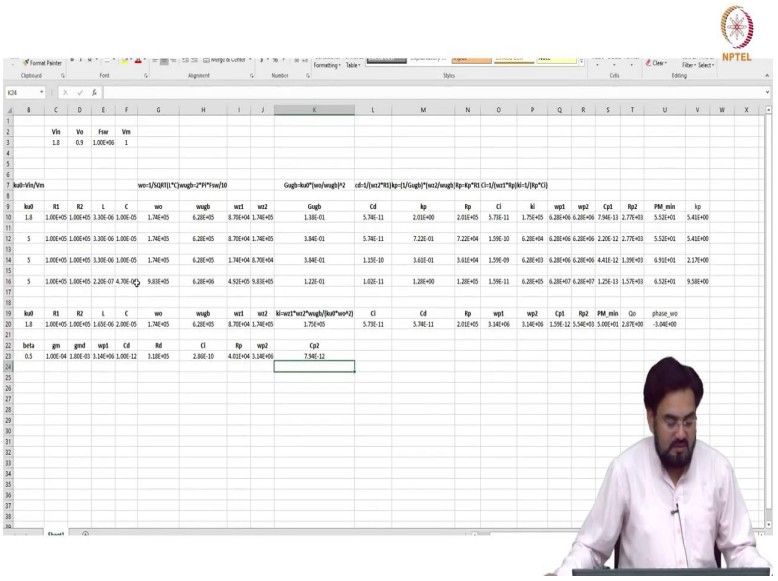
So, this is a linear model. When I go back to my switching model, I should be able to see a similar response.



The above image shows the switching model.

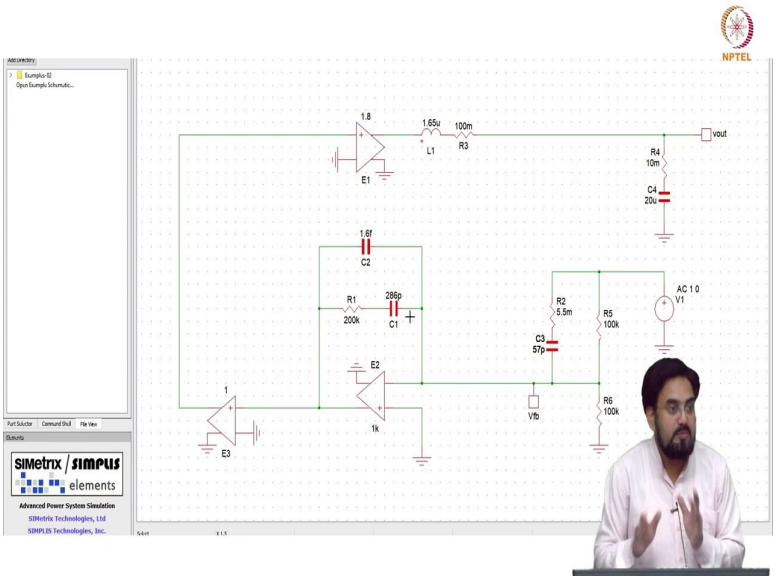


See, it seems almost the same behavior. The only thing you might see that your undershoot overshoot might be worse in this case compared to linear. Because now you are working on switching model. So, you are sampling. So, you have a clock delay, from the PWM it will introduce a delay and because of that delay, your transient response will be worse compared to what you are plotting in the linear.



So, this is what I was telling you guys to create a spreadsheet in excel and you fill all the values LC or k_{u0}, V_{in}, etc. The beta factor will only come into the picture if you are using a Gm-C compensator. So, we already did the calculation and used the formula for k_i. ω_{z1} and ω_{z2}, you can already decide where you want to place. ω_0 and ω_{ugb} will be known. So, the LC value will give you $\omega_{0,}$ and switching frequency divided by 10 will give you the ω_{ugb}.

So, C_i can be calculated from there because R_1 was the feedback resistor. So, that was a 100k and then, C_d your basically second zero capacitor can be calculated, R_p can be calculated based on your first zero or proportional gain. And then I am adding these two poles. These are high-frequency poles which are placed see you can see I am placing five times of ω_{ugb} H20 is nothing but omega_ugb. So, now we will see why exactly we need these two poles.



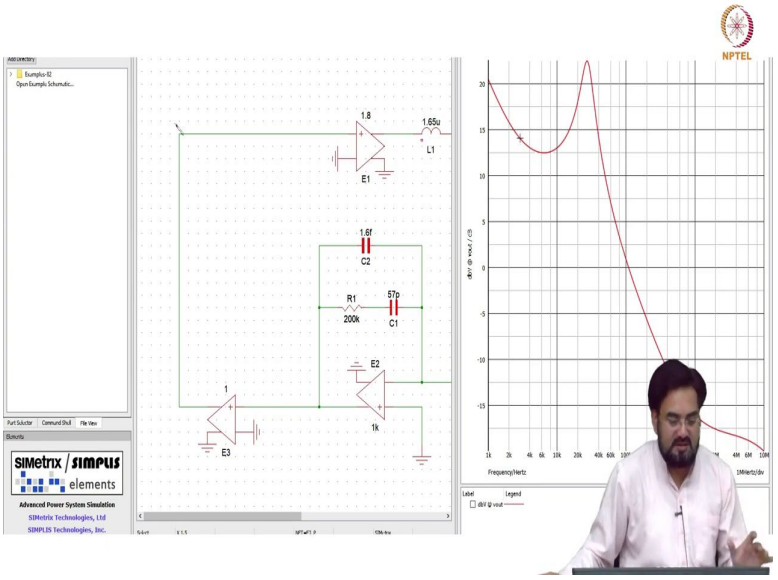
So, in order to add those two poles, We can add a resistor in series with C_d and a capacitor in parallel with C_i and R_p. If you do not have this resistor then at high frequency, this will get shorted. So, the gain will be infinite. Now, this resistor will limit your gain which means you are introducing a pole. Let us say I will make it femto which means I am just removing this cap. One thing you need to remember is that it should not affect your loop gain. That is why we are keeping these poles outside the ugb.

It may have some effect on your phase margin even if you keep it 5 times away. So, these two poles may cause a drop of maybe 10 degrees or so in the phase margin. Without these poles, you have to make sure that your phase margin is enough so that after adding this pole you still get a 55 to 60 degree kind of phase margin.

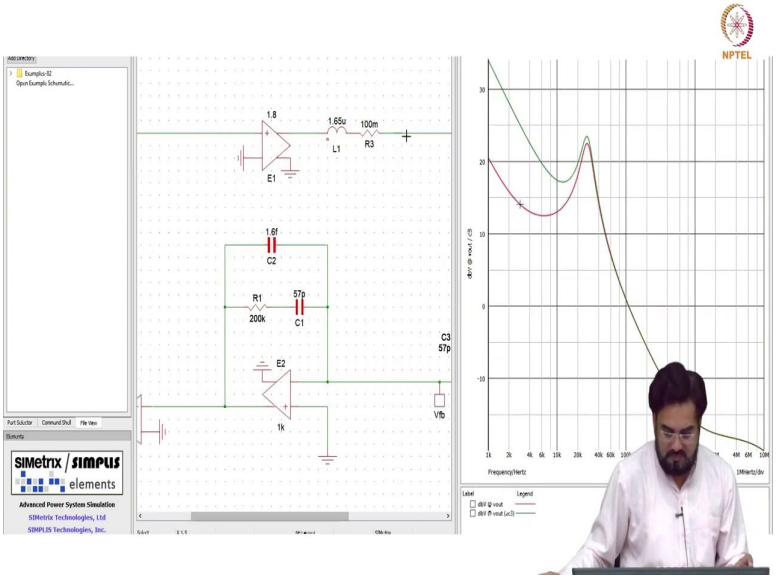
One thing I wanted to tell you guys that if you remember I mentioned to you that it does not matter where you place the first zero, your gain will automatically get adjusted if you use that particular formula. Let us say I moved my first zero inside. So, that will increase your proportional gain and your ugb will be shifted. So, now, k_i needs to be adjusted. So, if you change this capacitor C_1, which is an integral cap and this is also moving your zero inside.

So, no matter what the value of this cap is, your proportional gain is decided by R_1 and this feedback resistor. So, you are not affecting proportional gain here and that is why if you move your zero inside by simply changing this cap then it is affecting your integral gain also. So, your UGB will not get affected which means I can use any cap here. Smaller number or

higher number as long as I keep the proportional gain the same. So, I am using 286 Picofarad here.

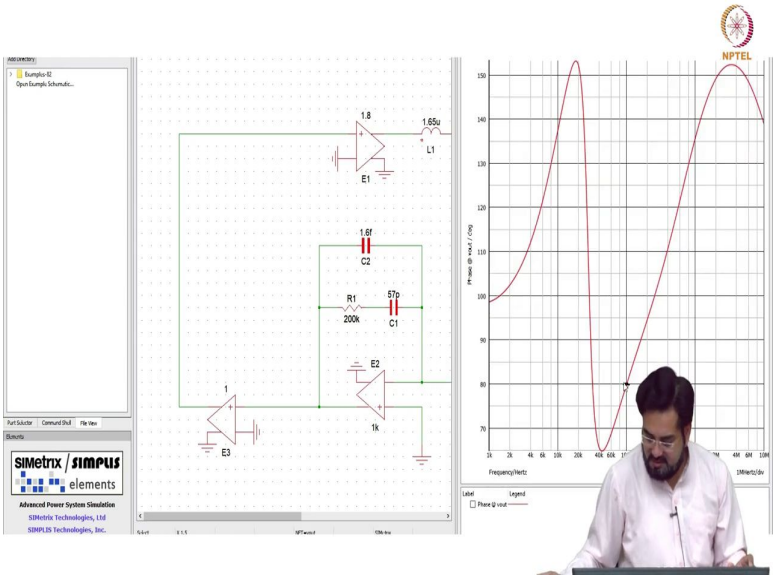


Which is giving me this kind of response. Now, if I make it 57 Picofarad which is the original value which we had. So, it will affect this shape, but the shape after ω_0 should not get affected or you can say that the ugb should cross at the same point.

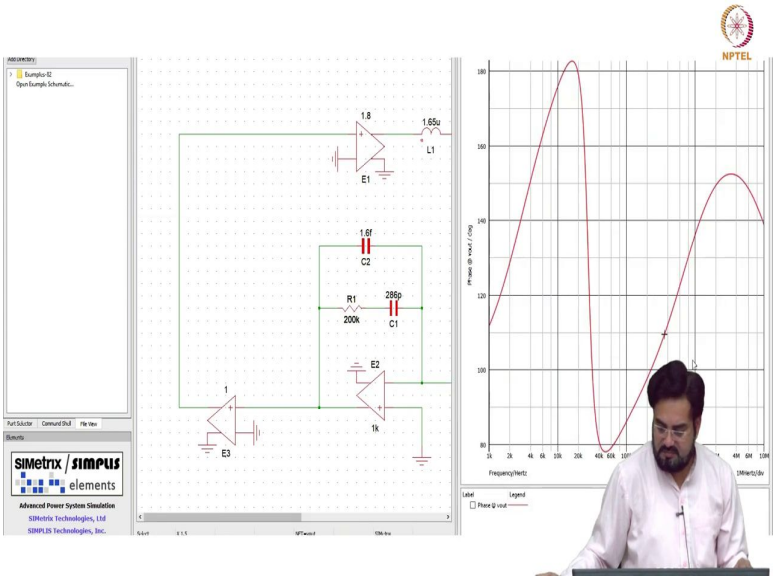


So, you can see here. Your gain is shifted because ω_{z1} is placed at a higher frequency which means you are placing ω_{z1} here when gain was dropped more but here you are placing early when gain was higher, so you needed to reduce the integral gain and that is what is

happening. The whole curve is shifted down before you place the first zero. But here, if you see 0dB, it remains the same and your phase margin should also be roughly the same.

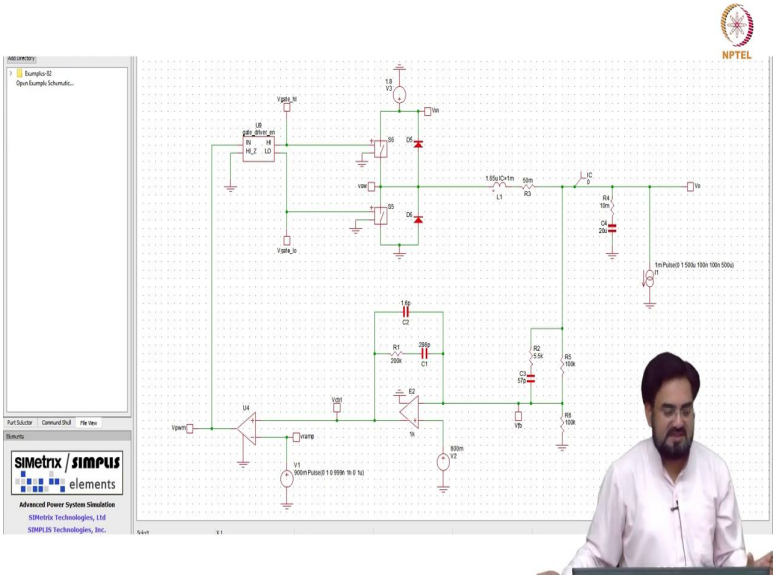


So, the phase margin is roughly 80 degrees we are getting here, and if I make it 286 pF.

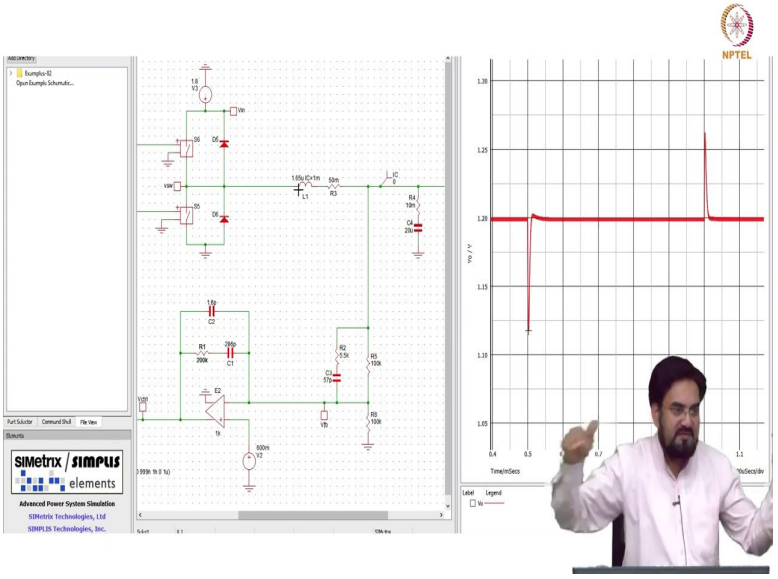


You will get a slightly higher phase margin here because the first zero is shifted at a lower frequency in this case which will increase the phase margin by a very small margin. The same thing will happen if you move the second zero at a lower frequency, your phase will be boosted because the phase contribution by this zero at ugb will be more. Because your separation between your ugb and that zero is more so that will add more phase at ugb.

So, you can improve phase margin by moving these two zeros at a lower frequency, but usually the first zero, we do not want to do that. First zero we have put on $\omega_0/2$. The second zero you can put at $\omega_0/2$ but moving that lower may not help much. I mean you may get maybe 2 or 3 degrees improvement in phase margin but there is a drawback with that. If I keep moving the zero inside then I have to add more caps. So, the area is the one problem; another problem is that the mid band gain is reducing. Your settling will be much lower compared to when you place the zero at a higher frequency. Because I mentioned that you want your loop gain to look like first order but moving inside means you are getting a flat gain in between and your settling will slow down and we can see that in simulation.

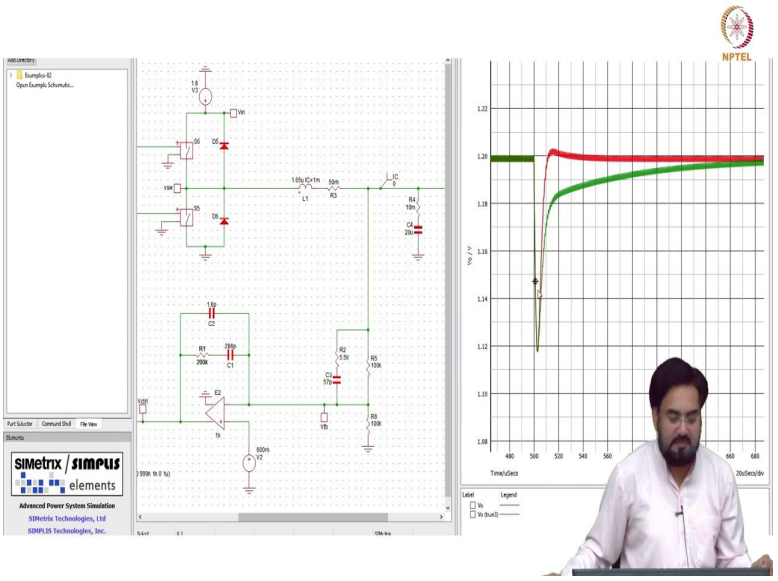


So, this is what I had. So, if you remember we change the inductor and capacitor. So, we can keep the same.

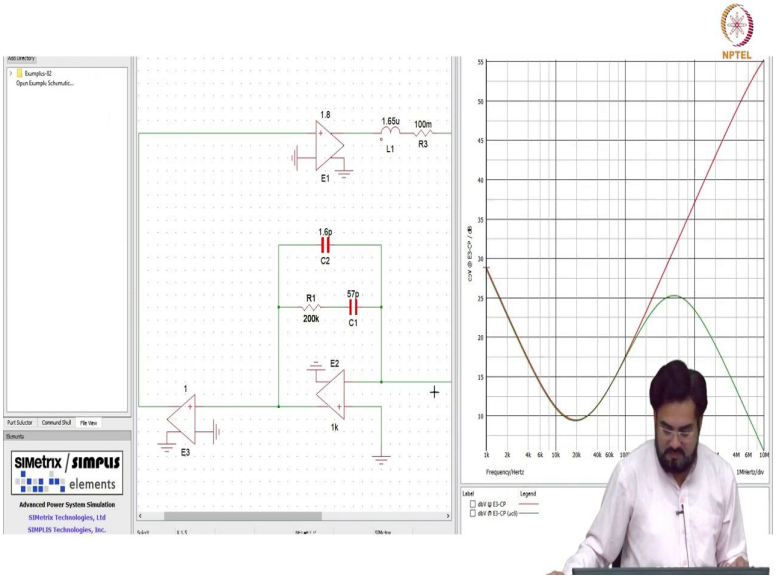


So, this is how it was looking. Now, I simply make it 286 pF which means ω_0 by 10. No, the curve means your ω_z shifted lower. So, it will be flatter for a wider frequency range. So, what do you have? You have an integrator then first zero, we will make it flat, then second zero will raise the gain. So, in between the flat if you move the first zero inside that you are expanding that region.

And if you move the first zero closer to ω_{z1} then you will more be getting like a narrow kind of that band. Now, you are widening that band. So, if you are looking at overall loop gain that will also flatten out for a wider range that will not look like a first order system in that case. So settling will not be good in that case and we can look here.



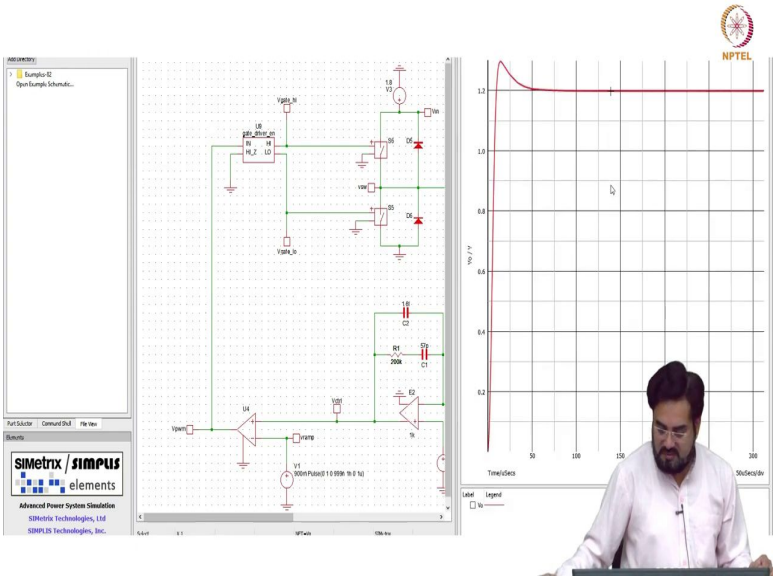
So, your undershoot will hardly get affected, but it will settle slower because of the lower gain in the mid band because that is flat for a wider range of frequencies and that is why settling is getting slower here. So, it is settling here, but this guy will take more time. So, if you take 1 percent or so, then this might take almost 100 microseconds to settle but this guy settles within 20 microseconds or so.



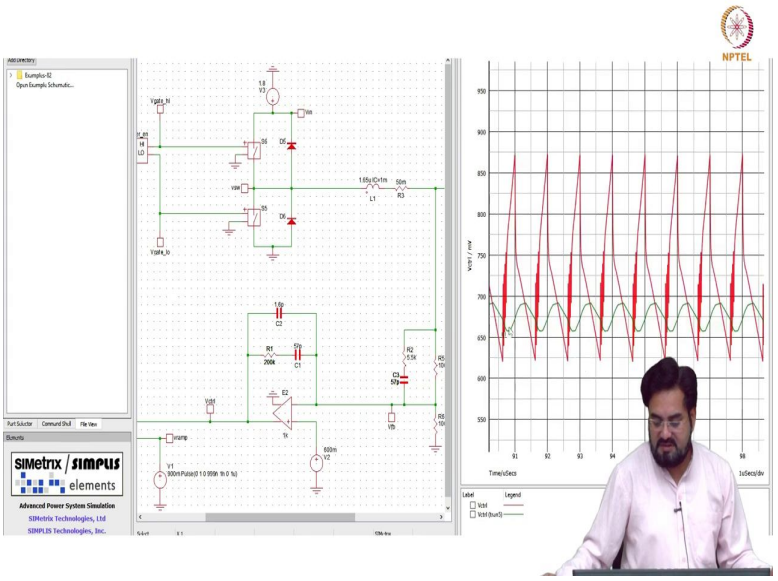
So, now, if I want to see in the case of 57 pF. Let us see what is happening here? So, without those two poles, there will be an integrator then first zero and second zero, the gain is rising. Now, if I increase this. So, I have added two poles now, let us see what happens. So, you have 3-poles and 2-zero. One integrator and two additional poles. So, it was rising. So, one

pole will cancel the zero and the other pole will cause minus 20 dB per decade. So, now, if I look at the gain at 1 megaHertz, here the gain is 23 dB; but here the gain is 37 close to 40 dB. So, maybe 7 to 8 times the difference. You can see and what is happening at 1 megaHertz?

So, you will see a large ripple being passed by this here and not only passed but it is getting amplified. This is also amplifying, but the amplification is reduced. We know that 1 megaHertz is 10 times higher than ω_{ugb}. So, even your loop will not suppress that. If it was a lower frequency, it would have been suppressed, but it will be fully passed. So, we can see the difference here 57 Pico. So, I will remove these poles and we will see how much ripple we are getting here, and then we will add the pole and see what we are getting.



So, output it settled drop voltage.



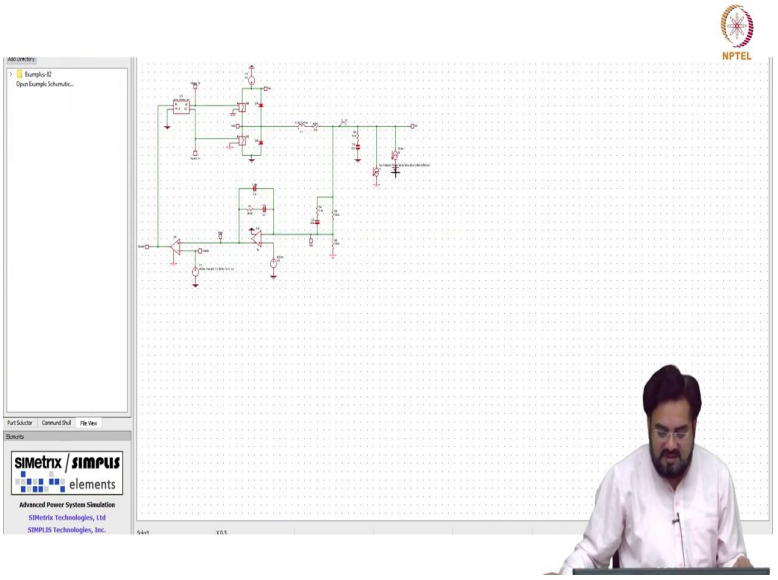
So, this is what we are getting here. Now, I will add these poles and see what happens to this. You can see a huge difference. So, why do we care about this ripple? It will not affect your duty cycle if you say, the reason is that ripple is coming at the same frequency as your PWM. So, your sawtooth will sample. So, your sawtooth and this. So, this comparator will sample. So, if you compare the saw tooth your control voltage. It will always cross at that same point. It does not matter how large the ripple is. Then, why do we care about this?

If this ripple is crossing at the same point every cycle, your duty cycle will not change, your switching frequency is the same. So, why would that affect your output ripple, it should not affect. V_{pwm} is not changing due to this.

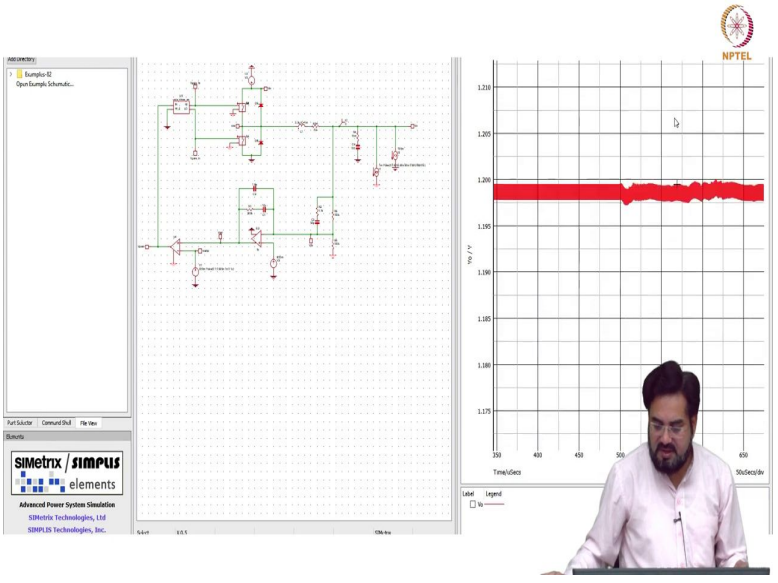
Let us say this is a PWM at 1 megaHertz and if I have a ripple injected in this output. Let us say at 1.01 megaHertz which means 10 kiloHertz higher. 1.01 megaHertz is still very high. So, it will get amplified and pass here and now every cycle if you look at 1.01 megaHertz and your sampling at 1 megaHertz. So, the control voltage will be changing every cycle. And you will see a tone at 10 kiloHertz. It is just like multiplying the two signals. If you have 1 megaHertz signal and take 1.01 megaHertz. You will get those 2 tones and you will get a difference of the two and the difference of the two will be sitting at 10 kiloHertz and 10 kiloHertz will not be suppressed by LC because that is very low. So, that should appear here.

But why would I have a 1.01 kiloHertz sorry megaHertz ripple here at the output? Think about you having a load here, it could be a switching load and the switching frequency of that

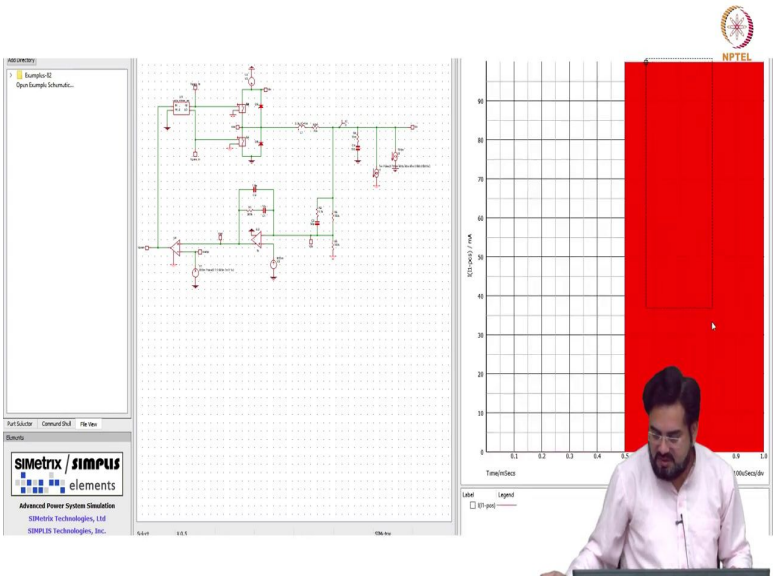
might be different. So, that may cause a noise here and that will get injected back then amplified and appear at the output. So, let us see what happens.

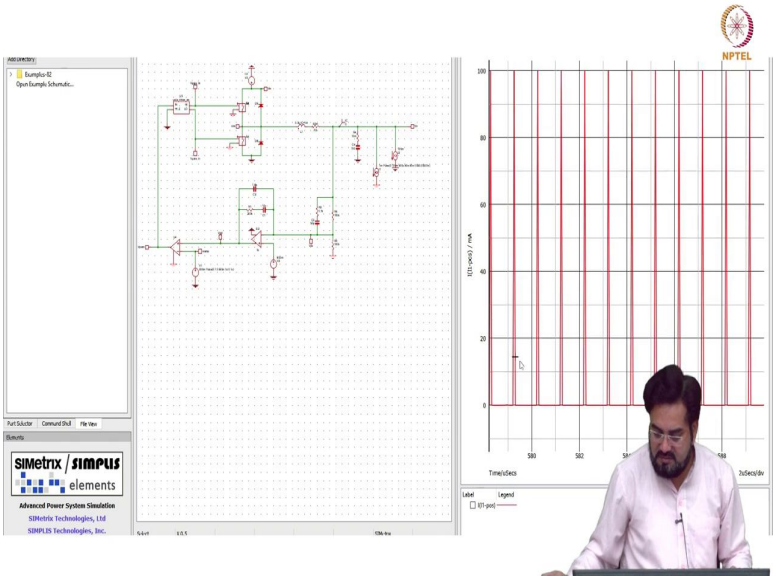


I have a 500 milliamp fixed DC load current. So, let us say some of the loads are DC and drawing DC current while some of the loads are switching and the switching load will obviously be a digital load. So, it will draw the current for a very short time. Just take the case of an inverter, during the transition only you get the current spikes.

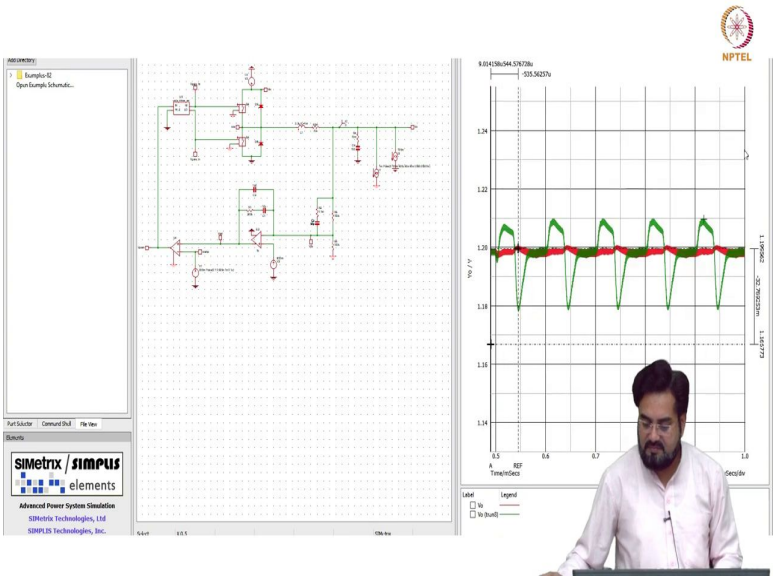


So, I will turn off this. So, you get a very clean output.



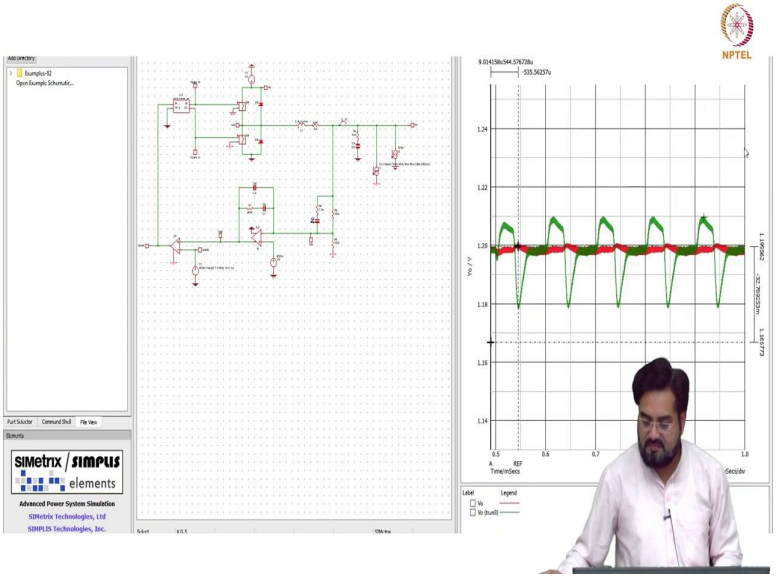


So, this is what I have. So, I have added current spikes that are going from 0 to 100 milliamp for a very short time. So, this should cause a ripple at the output and it should be visible in your output.



So, I am introducing that at 500 microseconds. So, you can see it here. So, the frequency of this I have set at 1.01 megaHertz. So, which means this should be at 10 kiloHertz. So, the peak to peak should be 10 kiloHertz and you can measure it. Now, this is with the pole added. Now, I will remove these poles and we will see what happens.

So, this does not look bad compared to your output without switching load because this is a very small ripple, but now if I do not have those poles drop. This is appearing at 10 kiloHertz and think about if you are driving an audio amplifier with this 10 kiloHertz and 10 kiloHertz is an audible range. So, you can listen to these tones in that case.



That is the significance of those two poles that we are adding at a higher frequency and some of this will get suppressed by the loop gain because this is appearing at low frequency. So, your bandwidth is 100 kiloHertz. Think about PSRR. So, anything below your ugb will be suppressed by the loop.