Power Management Integrated Circuits
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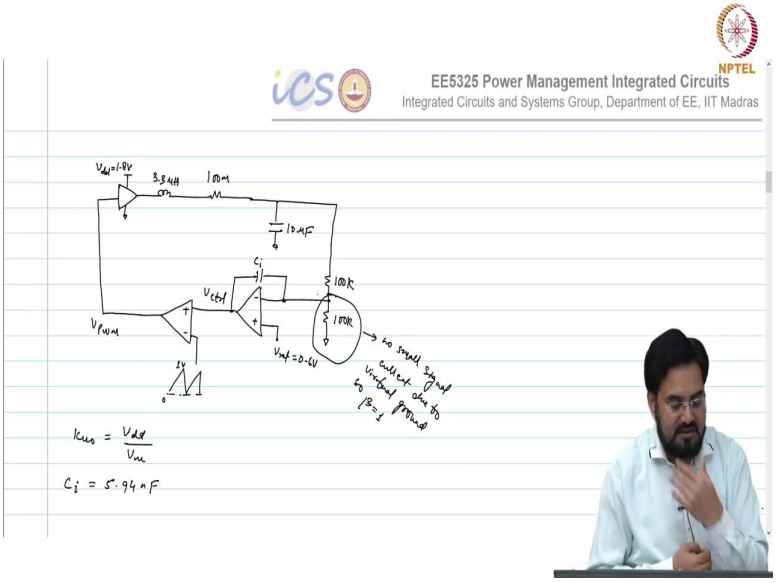
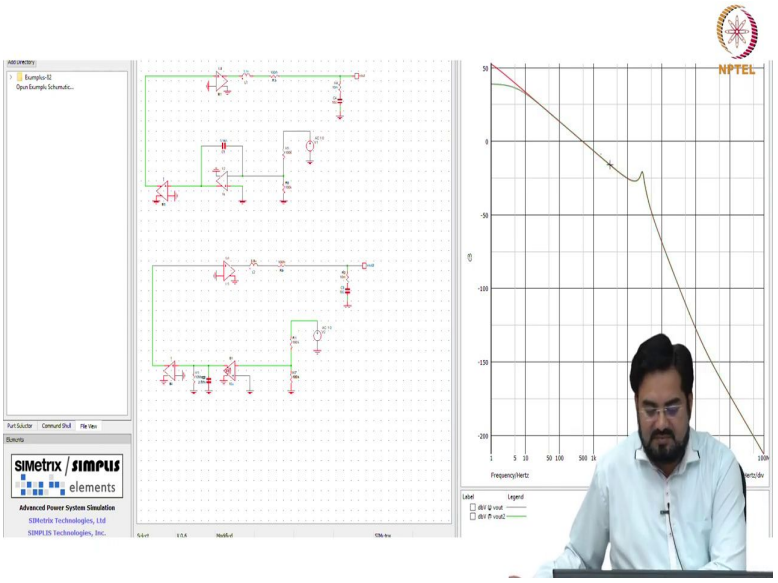
Lecture – 50
Dominant Pole Compensation (Type-I with Op Amp-RC Architecture)



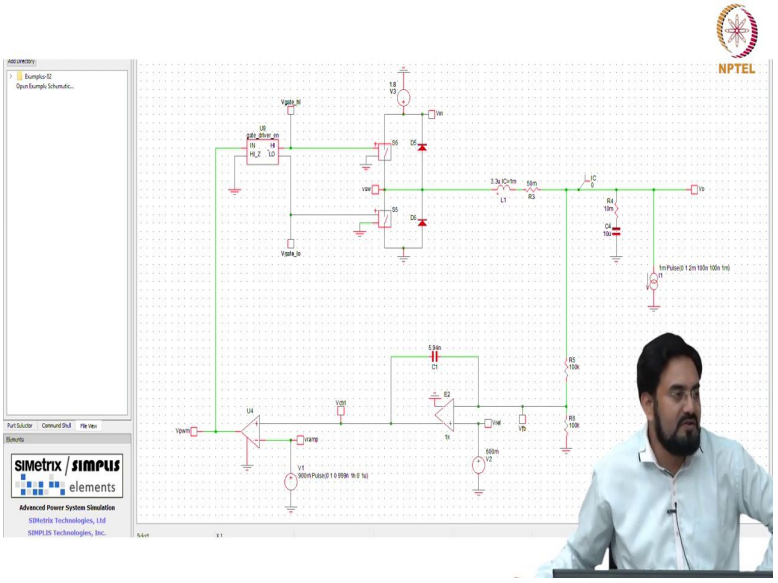
The circuit of the DC-DC converter using the Op-Amp RC integrator for dominant pole compensation is shown in the image above. We will only need a capacitor because we are using the feedback resistor in the integrator. □ factor will be one in this case because in the loop gain analysis both the terminals of the bottom feedback resistor are connected to the ground. K_{u0} will be V_{dd}/V_m here. If we look at the example in the previous lecture then K_i will be half the value in this case.

$$\frac{1}{RC_i} = k_i$$

Substituting R equal to 100kΩ and k_i equal to 6.734 krad/sec then the value of the C_i will be 5.94nF.

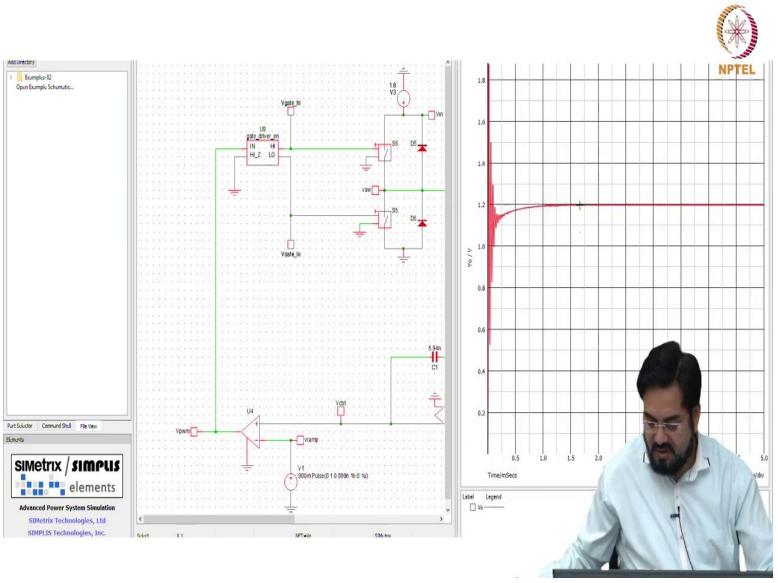


In the above image, we can see that the frequency response is the same for both Op-amp RC and Gm-C integrator when we use double the capacitor value in opamp RC compared to that of Gm-C.

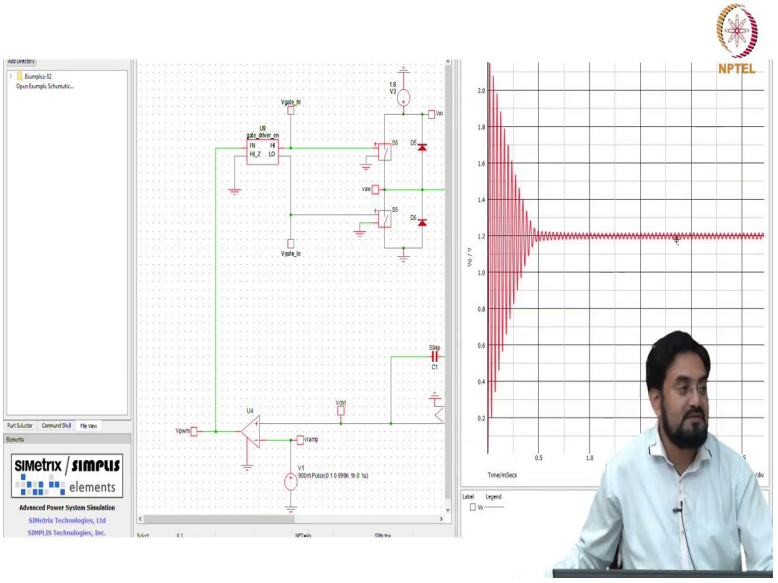


The above image shows the complete switching circuit of the DC-DC converter with the Op-Amp RC integrator.

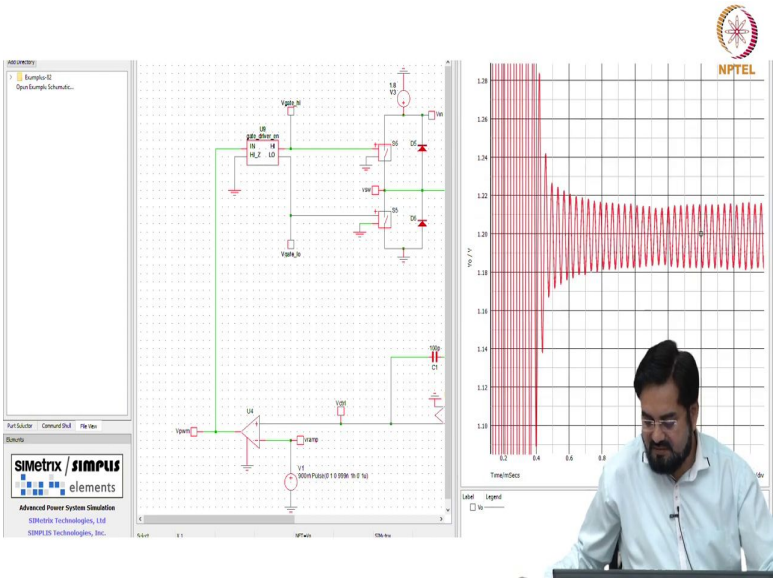
Output voltage should be stable in this case, it may have some weak ringing around resonance because we still have that peaking in the frequency response. If we do not want to see the ringing then we have to increase the gain margin more maybe minus 40 dB or so.



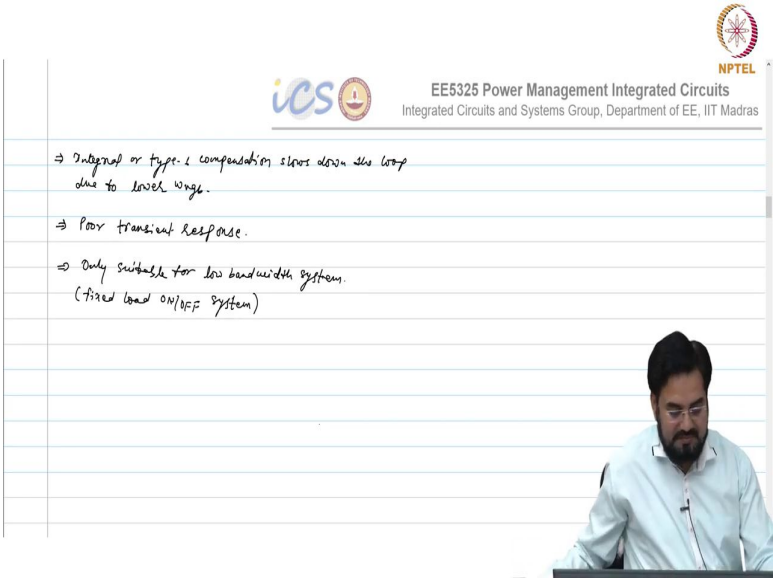
The above image shows the settled output voltage at 1.2V. The value of C_i we used was 5.94nF so that we can get -20dB gain margin.



The above image shows the output voltage for C_i equal to 594pF i.e. 0dB gain margin. We can see that the output is unstable.



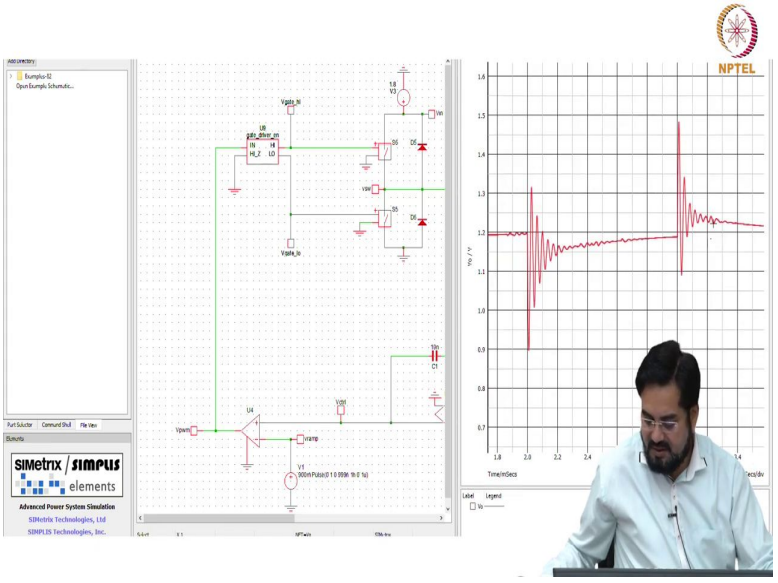
And if we further reduce C_i to 100pF to make gain at ω_0 more than 1. We can see that the output voltage oscillation magnitude increased.



Integral or type 1 compensation slows downs the loop due to lower UGB. We do not have any option here because to push the LC poles outside UGB and to have enough gain margin, we have to kill the bandwidth.

We will get a poor transient response in type I compensation. Loop will not respond very fast when we give a load line transient because it will take some time to change the control voltage which in turn changes the duty cycle slowly and the inductor current will change

slowly, which means the capacitor has to supply current for a larger duration and the output voltage will dip or rise more. The output voltage will undershoot or overshoot more and settling time will also increase because the loop is very slow.



In the above image, we can see the transient response. Ringing in the transient response is the resonant frequency. To decrease the ringing we have to increase C_i which will further reduce the UGB and make the transient response even worse.

Type I compensation is only suitable for a low bandwidth system. A fixed load system is a low bandwidth system. For example, a battery charger is a fixed load system because we usually charge a battery with a fixed current.

Type I compensation is simpler to implement because it requires only one capacitor but the capacitor value is large so most of the time with type I compensation we require an off-chip capacitor. In the case of a Gm-C integrator, we can reduce the Gm value to reduce the capacitor value required but then offset will increase because of low Gm value and increase the between V_{REF} and V_{FB}. In the case of a Gm-C integrator, we can reduce the capacitor value by increasing the value of feedback resistance and it will also affect the error between V_{REF} and V_{FB} but the area will increase on increasing the value of feedback resistance or we need to use off-chip resistance.