

Power Management Integrated Circuits
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Lecture - 49
Dominant Pole Compensation
(Type-I with Gm- C Architecture)

Dominant pole compensation


we use integrator or type-I compensation.


$$H_{comp}(s) = \frac{k}{s}$$

and push ω_0 outside ω_{ugb}

Gain at ω_{ugb} is $> 0\text{dB}$ & $pm \approx 0 \rightarrow \text{unstable}/q$.

$$\omega_{ugb} = \frac{\omega_0}{Q}$$





In Dominant pole compensation, we use $H_{COMP}(s)$ as an integrator or type I compensator. So, $H_{COMP}(s)$ will be equal to k/s and we will push ω_0 outside ω_{ugb} . How far we need to push ω_0 outside ω_{ugb} depends on the Q factor.

Let us say we make ω_0 equal to ω_{ugb} . If there is not any Q factor then gain should have crossed 0dB at ω_{ugb} but due to the Q factor gain at ω_{ugb} does not remain 0 dB and its more than 0db and the phase there is almost touching -180° . The system is unstable because gain at ω_{ugb} is more than 0dB and the phase margin is almost zero.

$\omega_{ugb} = \frac{\omega_0}{Q_0}$

unstable because gain = 0dB at ω_0 (phase margin = 0dB)

$\omega_{ugb} < \frac{\omega_0}{Q_0}$
 for -20dB gain margin
 $\omega_{ugb} = \frac{\omega_0}{10Q_0}$

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Let us say we make ω_{ugb} equal to ω_0/Q_0 . Gain at ω_{ugb} will be 0dB but gain at ω_0 will also be 0dB because of the Q factor and phase at ω_0 will be almost -180° . The system is again unstable because the gain at ω_0 is more 0dB and the phase margin is almost zero. Gain at ω_0 equal to 0dB means gain margin is 0dB. So for a stable system ω_{ugb} should be less than ω_0/Q_0 and for -20dB gain margin ω_{ugb} should be equal to $\omega_0/10Q_0$.

$\frac{V_o(s)}{V_{in}(s)} = L_{hcomp}(s) = \beta H_{amp}(s) H_{comp}(s) H_{LC}(s)$
 $= \beta \frac{k_i}{s} \frac{V_{dd}}{V_{th}} H_{LC}(s)$
 $\beta \frac{V_{dd}}{V_{th}} = k_{uo}$
 $L_{hcomp}(s) = \frac{k_{uo} k_i}{s} H_{LC}(s)$
 $k_{uo} k_i = \omega_{ugb} = \frac{\omega_0}{10Q_0}$
 $k_i = \frac{\omega_0}{k_{uo} 10Q_0} = \frac{1}{10k_{uo}} \left(\frac{R_{dso}}{L} + \frac{1}{R_{load}C} \right)$

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Putting the value of $H_{COMP}(s)$ in $LG_{COMP}(s)$.

$$LG_{COMP}(s) = \beta \frac{k_i}{s} \frac{V_{dd}}{V_{th}} H_{LC}(s)$$

Assume

$$k_{u0} = \beta \frac{V_{dd}}{V_m}$$

then

$$\omega_{ugb} = k_{u0} k_i = \frac{\omega_0}{10Q_0}$$


We know the value of ω_0 and Q_0 . So from the above equation, we can find the value of k_i .

$$k_i = \frac{1}{10k_{u0}} \left(\frac{R_{LOSS}}{L} + \frac{1}{R_{LOAD}C} \right)$$

For No load

$$k_i = \frac{1}{10k_{u0}} \times \frac{R_{LOSS}}{L}$$

We will be modeling the sample system in continuous time because it is easy to model in continuous time. We will first design in the continuous model according to the specifications then convert it into sampled system. In the dominant pole compensation case we have to find the value of k_i .



For no load,
 $R_{LOAD} = \infty$

$$k_i = \frac{1}{10k_{u0}} \left(\frac{R_{LOSS}}{L} \right)$$

Example

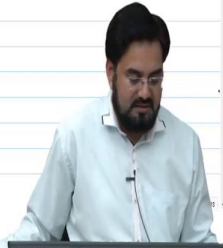
$V_{dd} = 1.8V$, $V_{th} = 1.2V$, $V_{ref} = 0.6V$
 $F_{bw} = 1MHz$, $L = 3.3\mu H$, $C = 10\mu F$
 $R_{dsn} = 50m\Omega$, $R_{dcr} = 50m\Omega$, $V_m = 1V$

$$k_{u0} = \frac{V_{dd}}{V_{th}} \times \beta = 1.8 \times \frac{1}{2} = 0.9$$

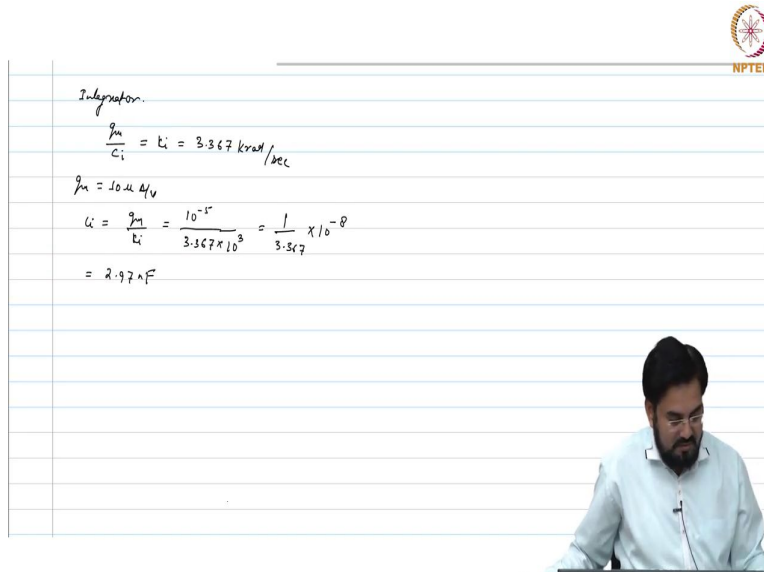
$$R_{loss} = R_{dsn} + R_{dcr} = 100m\Omega$$

$$L = 3.3\mu H$$

$$k_i = \frac{1}{10 \times 0.9} \left(\frac{0.1}{3.3\mu H} \right) = 3.367 \text{ krad/sec}$$



In the example in the above image value of k_i in no load condition is calculated and its value is 3.367 krad/sec.



Integration.

$$\frac{g_m}{C_i} = \omega_i = 3.367 \text{ krad/sec}$$

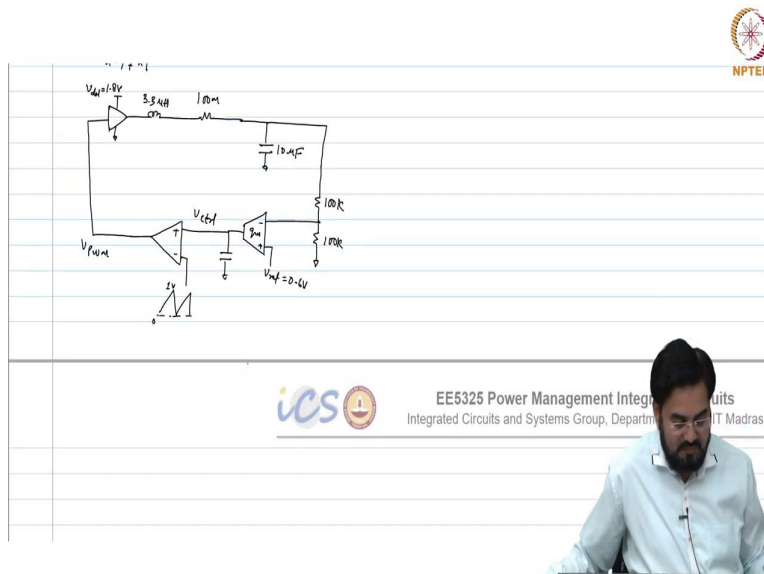
$$g_m = 10 \mu\text{A/V}$$

$$\omega_i = \frac{g_m}{C_i} = \frac{10^{-5}}{3.367 \times 10^3} = \frac{1}{3.367} \times 10^{-8}$$

$$= 2.97 \text{ nF}$$

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If we use Gm-C integrator with g_m of 10 $\mu\text{A/V}$ for k_i of value 3.367 krad/sec then we will need a capacitor of value 2.97nF.



The circuit diagram shows a Gm-C integrator. It consists of an input stage with a differential pair of NMOS transistors. The input signal V_{in} is applied to the gates of these transistors. The sources are connected to ground. The drains are connected to a common source node, which is also connected to a load capacitor C_i . The output of the integrator is taken from this common source node. The circuit is biased with a supply voltage $V_{DD} = 1.8\text{V}$. The load capacitor C_i is 2.97 nF. The output voltage V_{out} is 0.4V. The circuit is implemented in a 0.18 μm CMOS technology.

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The above image shows the final circuit.