Power Management Integrated Circuits
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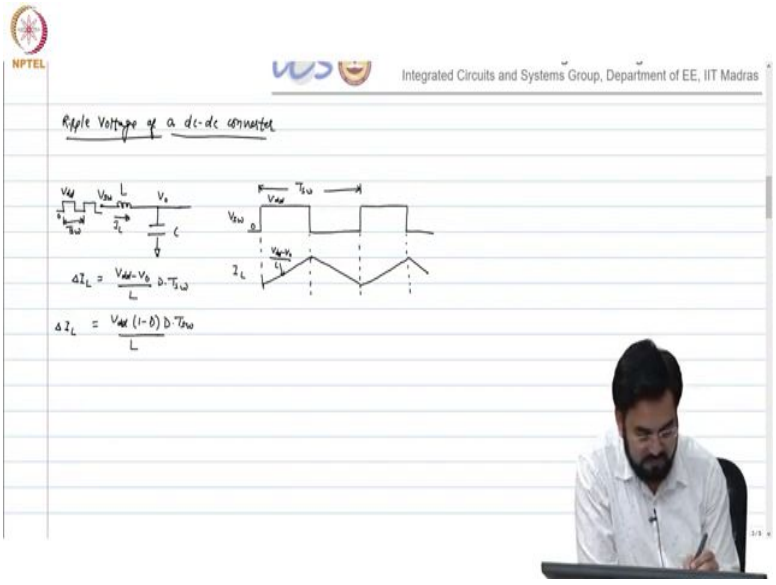
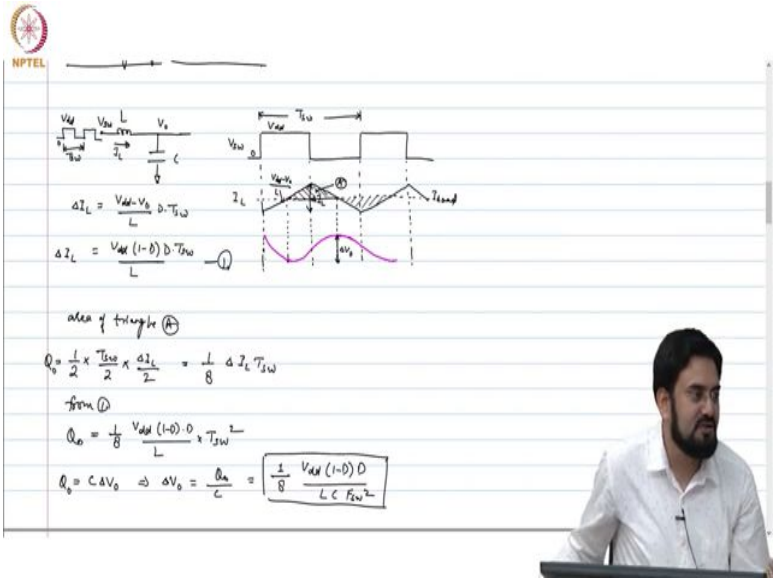
Lecture – 40
Output Voltage Ripple of a Buck Converter



Ripple current in the inductor of the DC-DC converter is

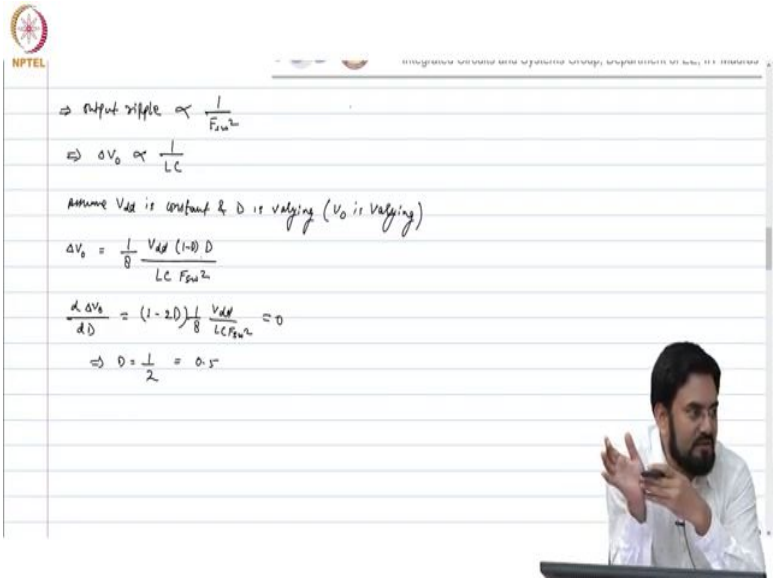
$$\Delta I_L = \frac{V dd(1-D)D}{L} T_{SW}$$

Whether there is a load or not, it does not matter because the ripple current will not get affected. The only difference is that the offset of the ripple current will change based on the load current. So, if we are only interested in ΔI_L then we can assume load current to be 0.



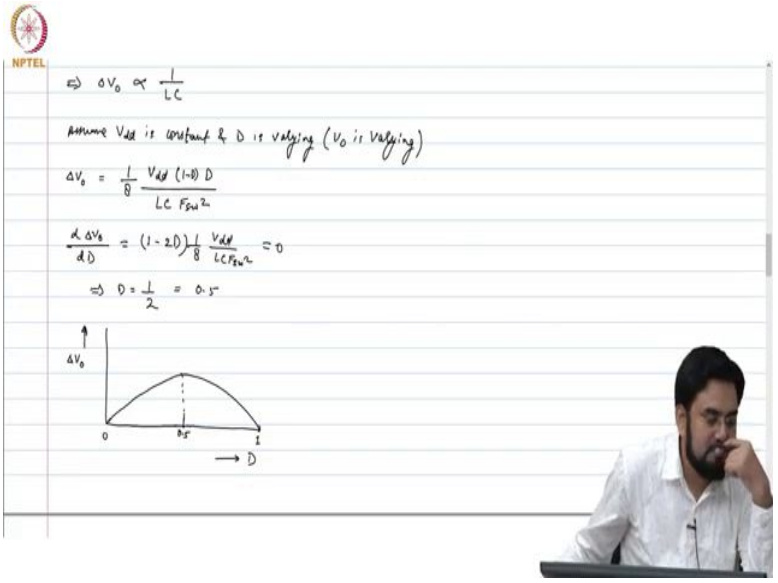
Waveforms of V_{SW}, I_L, and V_0 is shown in the above image. Since ripple current is going in the capacitor and we know that current is equal to C dv/dt, so which means current will get integrated and convert into voltage. So, we will get a parabolic kind of function at the output voltage. Inductor current will charge the capacitor when it is more than load current and discharge the capacitor when it is below load current. So, the peak and valley of V_o will come at the points where I_L is intersecting with the load current.

The area of triangle A in I_L waveform as shown in the above image is the amount of charge we are dumping into the capacitor while it's charging. If we divide the charge with the capacitance value then we will get peak to peak ripple value of the output voltage. The derivation for finding the peak to peak ripple value of the output voltage is shown in the above image.

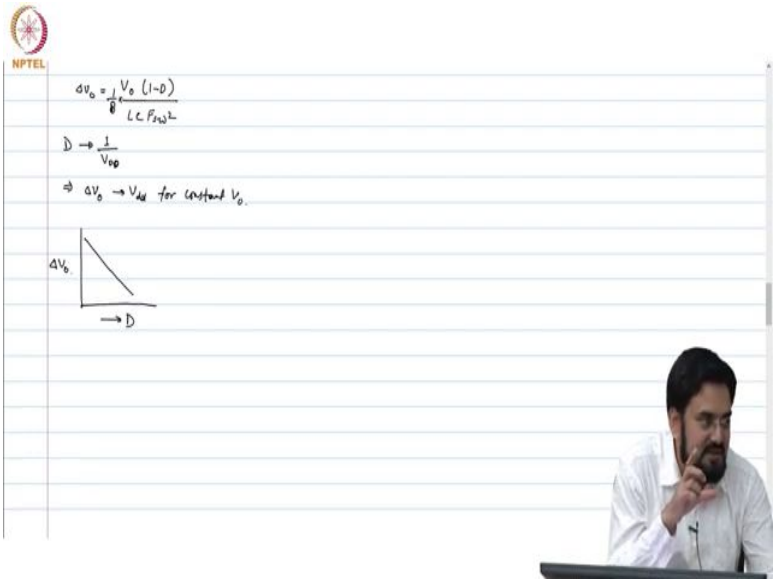


Output ripple is inversely proportional to the square of the switching frequency, inductance value, or capacitance value. If we increase the switching frequency, we get double the advantage compared to increasing the value of either inductor or capacitor. If we want to keep the output ripple constant and decrease the value of the inductor or capacitor then we have to increase the switching frequency that is why when we target let us say order of 10s of MHz switching frequency, the only intention is to reduce the size of inductor and capacitor. So, that size of the external components reduces, and the overall module size is reduced. We get the benefit in terms of transient response also because a higher switching frequency means we can have higher bandwidth.

Let us assume that Vdd is constant and D is varying which means V_0 is varying. To find the maximum value of output voltage ripple, we have to differentiate the output voltage ripple with respect to D. The calculation is shown in the above image. Output voltage ripple is maximum at 50% duty cycle.



The plot of ΔV_0 vs D is shown in the above image. There is a perfect symmetry around D equal to 0.5. At D equal to 0 and 1, output ripple will be 0, because one of the switches will be permanently off and it will not be switching at all. So, that is why both ripple current, and ripple voltage are 0 there. Inductor ripple current vs D curve shape is also same as the above curve and ripple current will also peak at D equal to 0.5.



If V_0 is constant and V_{in} (Vdd) is changing then we can write ΔV_0 as

$$\Delta V_0 = \frac{V_0 (1-D)}{8LC F_{SW}^2}$$

D is inversely proportional to Vdd for constant V_0. This implies ΔV_0 is proportional to Vdd for constant V_0. Maximum ripple will be at D equal to zero but at D equal to 0 there will no switching so we will start the ΔV_0 vs D curve at D value which is slightly greater than zero. Plot of ΔV_0 vs D is shown in the above image. On increasing D, ΔV_0 is decreasing or we can say that ΔV_0 is increasing on increasing Vdd. Same is the case for inductor ripple current And that is why when we keep increasing the Vdd we need an inductor which has a higher saturation current because the peak current will be load current plus half of the ripple current and at higher Vdd that is high. So, we need higher saturation inductor for higher Vdd.