Power Management Integrated Circuits
Dr. Qadeer Ahmad Khan
Department of Electrical Engineering
Indian Institute of Technology, Madras

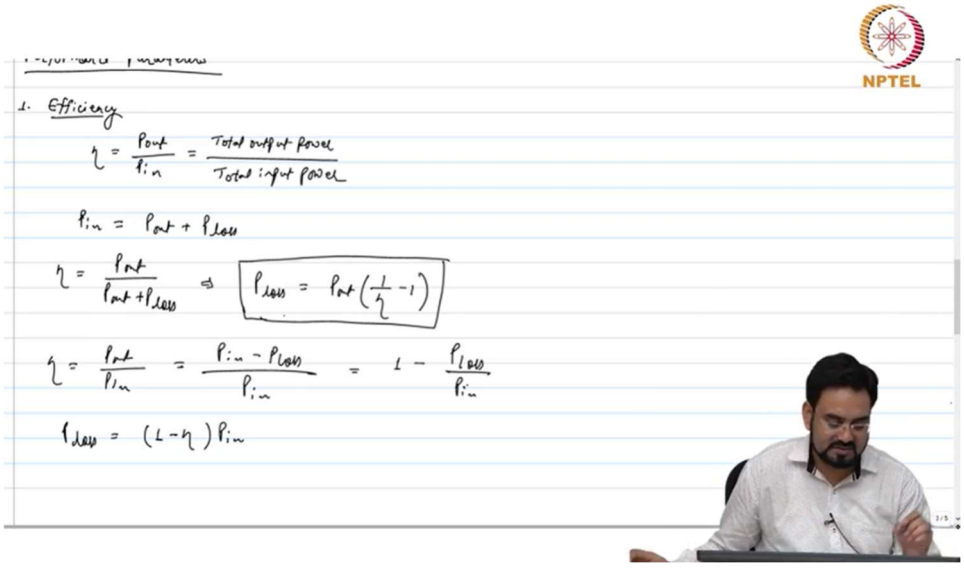
Lecture - 04
Performance Parameters of Regulators

Performance Parameters:

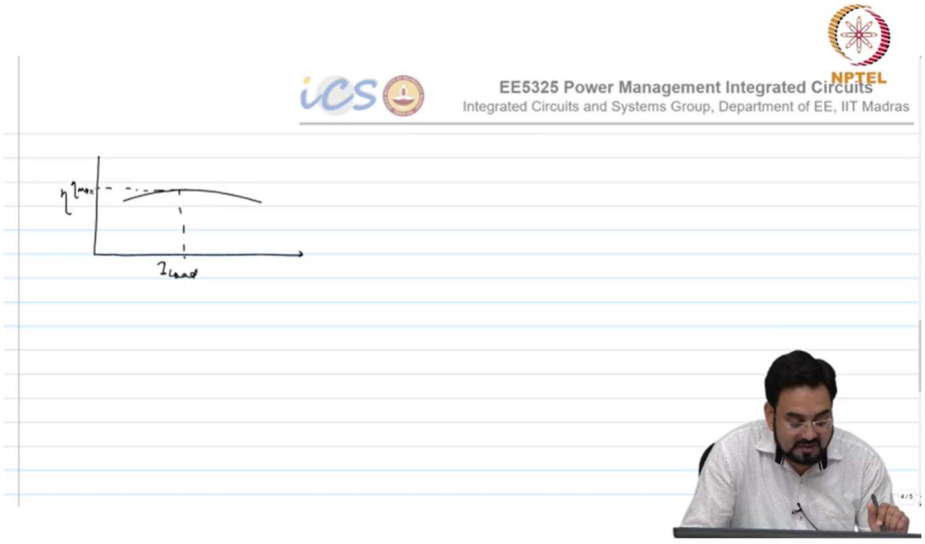
There are certain parameters based on which we measure the performance of any regulator whether it is a switching or a linear.

1. Efficiency: It is measured by the formula $\eta = \frac{\text{total output power}}{\text{total input power}} = \frac{P_{out}}{P_{in}}$

Power loss is given by $P_{loss} = \left(\frac{1}{\eta} - 1\right) P_{out}$ and the derivation is shown in below figure.



So, efficiency curve in most of the cases is measured with load current. In case of switching regulator efficiency curve mostly looks like flatter as shown in below figure. It will peak in some mid-range and as you keep increasing the load current, your I^2R losses will increase. So, efficiency will keep dropping. You get maximum efficiency at maximum I_{load} for which we sized our power FETs. And at light load and higher load it may reduce.

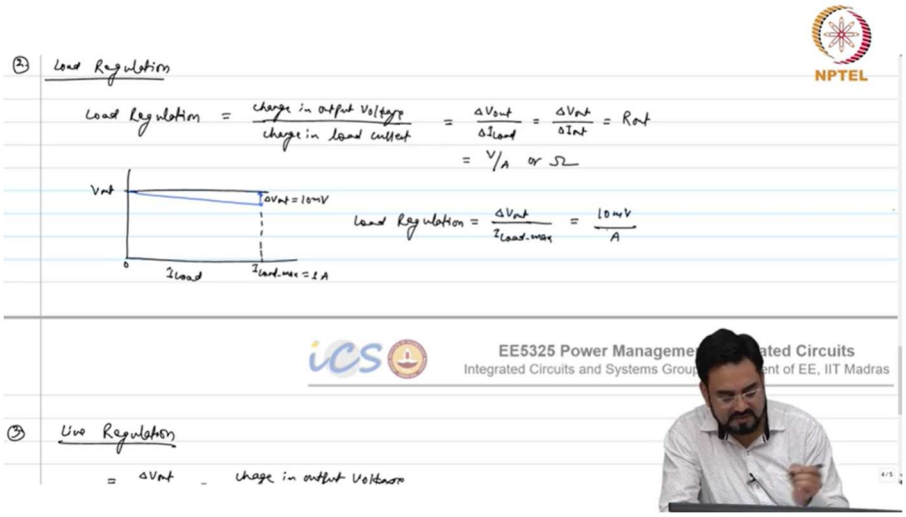


So, it will peak in a certain range of the load current. And most of the cases, we target maximum efficiency of 90% or above in switching regulators. In a linear regulator, your efficiency curve is different. In most of the cases it may be shifted down based on your dropout voltage or it may go even higher than switching regulator if dropout voltage is very less.

2. Load regulation: It is defined as

$$\text{Load regulation} = \frac{\text{change in output voltage}}{\text{change in load current}} = \frac{\Delta V_{out}}{\Delta I_{out}} = R_{out}$$

Where R_{out} is the small signal output resistance. So, we can say it is $^{V}/_{A}$ or Ω.

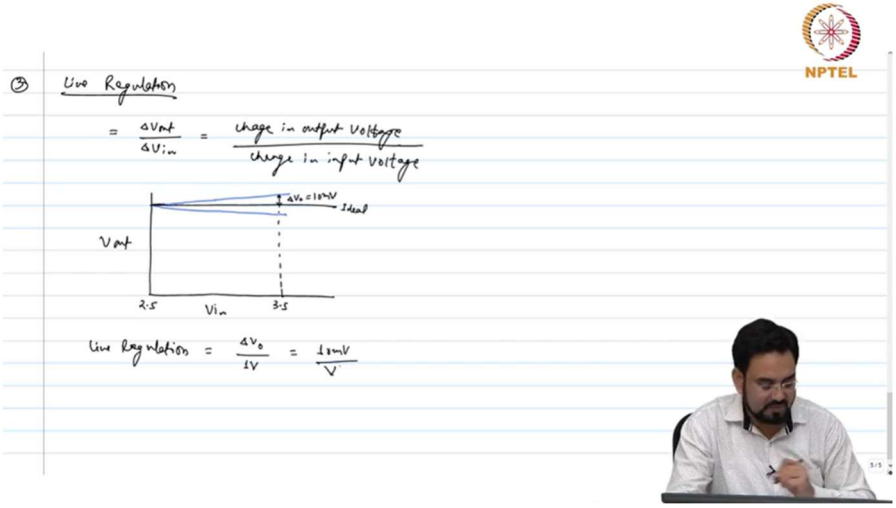


We do not want output to change when the load is changing. Ideally, I want R_{out} to be zero and that's why we say like ideal supply has zero output impedance, that is what it means because it will give constant voltage across any load current. Ideal and non-ideal plots are shown in the above figure with an example. And blue curve is non-ideal.

$$\text{Load regulation} = \frac{\Delta V_{out}}{\Delta I_{out}} = R_{out} = \frac{10\text{mV}}{1\text{ A}} = 10\ \text{m}\Omega$$

3. Line regulation: It is defined as

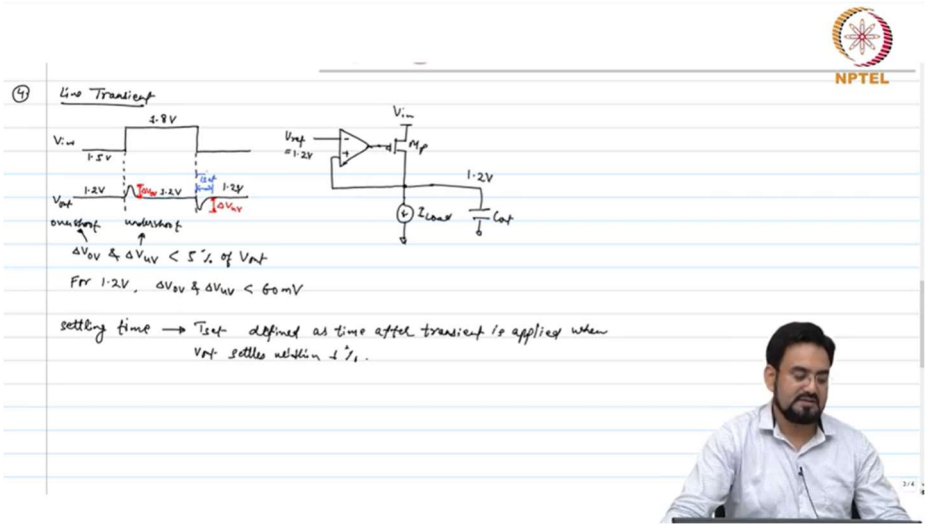
$$\text{Line regulation} = \frac{\text{change in output voltage}}{\text{change in input current}} = \frac{\Delta V_{out}}{\Delta V_{in}}$$



Ideal and non-ideal plots are shown in the above figure with an example. And blue curve is non-ideal. So, it may be in both the directions positive or negative we do not know, it all depends on design.

$$\text{Line regulation} = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{10\text{mV}}{1\text{ V}}$$

4. Line transient: Let's say V_{in} is not fixed but changing as shown in below figure. It is going from 1.5 V to 1.8 V. Now, let's say output is regulated at 1.2 V.



We will take an example of this linear regulator. When V_{in} changes, this past transistor will create a V_{gs} difference because this gate voltage cannot change instantaneously. So, the current in the output will increase and this will try to overshoot.

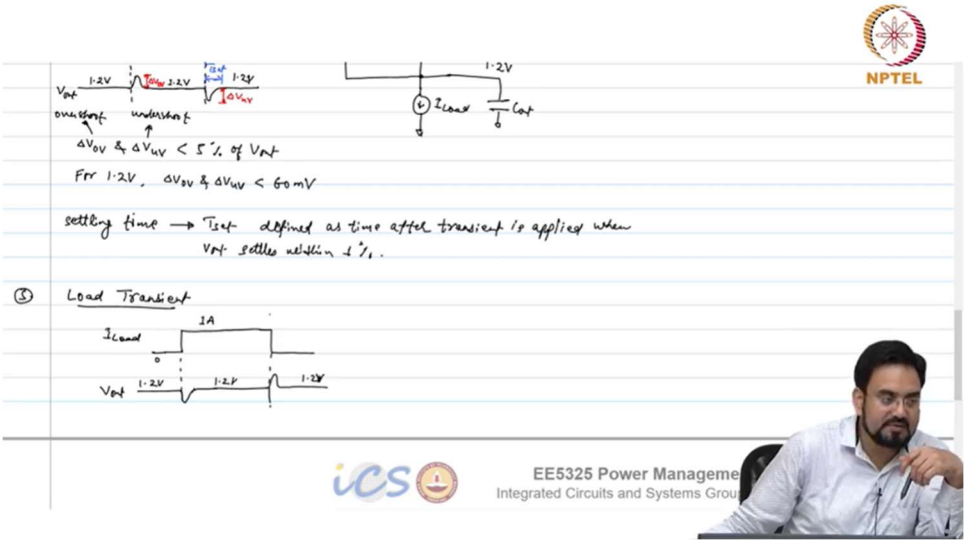
And since it is a feedback system, the feedback will try to recover and the recovery time will depend on your bandwidth. Since it has a finite bandwidth, this gate voltage cannot instantaneously change. Depending upon how fast your loop is, this overshoot will be determined. And then it will come back and then we restart regulating at 1.2 V again. Now the same thing will happen when it goes from 1.8 to 1.5 V. Now we are reducing, so output voltage has to reduce. So, output will dip and then try to recover.

So, you will see a undershoot (ΔV_{uv}) and overshoot (ΔV_{ov}). Most of the systems have specifications for regulated output voltage. Most of the system can afford ±10% variation in the output voltage but that 10% includes everything: your error, your line transient and load transient.

So, specification for transients is defined within 5% or less so that you keep the rest 5% margin for other errors. And when I say this 5%, this ΔV_{uv} and ΔV_{ov} should be less than 5% of output voltage. Which means for 1.2 output voltage, this ΔV_{uv} and ΔV_{ov} should not be more than 60 mV.

Other than this under shoot, over shoot we have another transient spec called settling time (T_{set}). It is defined as the time after transient is applied when V_{out} settles within 1% of the desired voltage.

5. Load transient: It is similar to your line transient. The difference is instead of changing V_{in} we change load here. And I_{load} is applied as shown in below figure.



All of a sudden when you apply the load current, this MOSFET has to increase the current in order to hold the output voltage. But due to limited bandwidth the same problem will happen again. That current can't change suddenly and all the load current for a very short duration or the duration for which your loop recovers will be supplied by your output capacitor and capacitor will start discharging. And then recover back again and the same thing will happen when you release the load. When you release the load, the MOSFET current will get dump into that capacitor and it will cause overshoot.

So, this under shoot, overshoot obviously in both the cases will depend on the bandwidth and value of the output capacitor you put. Let's say once my bandwidth is set, I want to further reduce then the only way is to increase the output capacitor. Another thing we need to remember in both line transient and load transient is this under shoot, overshoot will also depend on how fast you change the input or load current.

Let's say for line transient, I am changing line voltage from 1.5 V to 1.8 V in 10 nanoseconds. So, that is a very fast change. My bandwidth cannot respond or this feedback loop cannot respond that fast. But let's say if I make this change in order of 10 microsecond or so. Now this change is very slow and this feedback will track because it is not very fast and you will hardly see any under shoot or overshoot in the output. So, it all depends how fast you are changing.

So, if your change is much faster, then this under shoot and overshoot can only be reduced by increasing the output capacitor or increasing the bandwidth. But once you have designed your regulator, bandwidth is fixed and the only way to improve the transient response is by increasing the output capacitor.

6. Power supply rejection ratio:

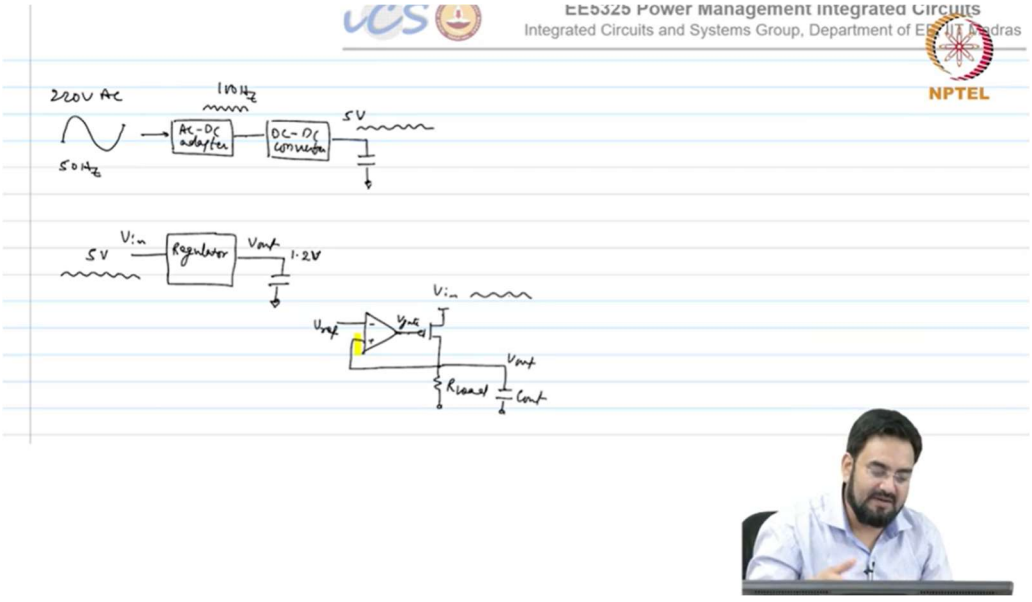
It is defined as PSRR = $\frac{\Delta V_{out(ac)}}{\Delta V_{in(ac)}}$

$$\text{PSRR (dB)} = 20 \log_{10} \frac{\Delta V_{out(ac)}}{\Delta V_{in(ac)}}$$

Line regulation is for DC and if you define it for AC then it becomes PSRR.

One example could be let's say take the case of a battery charger. We have 220 V AC 50 Hz, then it goes to your adapter. At the output of adapter frequency is 100Hz and it goes to your DC-DC converter. The output of DC-DC converter is regulated to 5 V which goes to your USB and it will also have some ripple.

But this DC-DC is switching at much higher frequency, maybe 1 MHz and it will have a high frequency ripple. It may have some portion of this 100 Hz component also but it's a very low frequency and your loop can track that. But when you have high frequency ripple, your loop will not respond to that and that will start appearing at your output.



If you remember, for line transient you made a sudden change in the line voltage and your loop can't respond that fast and you will see undershoot or overshoot in the output. It's only because your loop has limited bandwidth. So, the same thing applies here also. The only difference is instead of a step, now you have more like a sinusoid ripple but the concept remains the same. If this frequency component is so high that your loop cannot track, then that component will appear at the output of your regulator.

Now, this is your linear regulator which takes 5 V and gives you let's say 1.2 V output. This 5 V input is not clean and it has some ripple which could be anything like maybe 10 mV or 20 mV depending upon the converter specifications and the value of the output capacitor kept at the output of DC-DC converter. So, what all can be done to improve this PSRR?

Increasing the output capacitor can improve the PSRR, but that is not always true. It depends how you have designed your regulator. If your gate pole is dominant, then your bandwidth is limited by that pole not with the output capacitor. So, increasing the C_{out} may not help here until and unless you make output pole dominant. If you make the output pole dominant, then it will always help because you will get a direct filtering from input to output and it will behave like a low pass filter. So, making the low pass filter bandwidth lower and lower will reject more high frequencies and that will help.

So, there are two ways to improve the PSRR.

1. One is you just filter it out through the capacitor which is only possible if you make the output pole dominant.

2. If output pole is not dominant (gate pole is dominant) then increase your system bandwidth. Since it is a feedback system, if there is any change in the output your feedback will try to correct it. When it sees any ripple in the output it will try to change the gate voltage of the FET in such a way that nothing appears across V_{gs}.

If your bandwidth is very slow and it is not tracking the change in V_{in} then all the AC component which is appearing at the V_{in} will get amplified by the g_m of this PMOS and appear at the output. So $g_m R_{out}$ is the gain actually. So, this is looking like a common gate amplifier and everything will appear at output and it will make it even worse because this is acting as an amplifier.

So, now if I increase the bandwidth in such a way that let's say ripple is at 100 KHz and my bandwidth is 1 MHz which means 100 KHz can be easily tracked. If there is any change in the output, then your output will be fed back and at the same time it will try to change the gate voltage. Let's say V_{in} changes by a ±10 mV then feedback will try to change the gate voltage of PMOS in such a way that AC variation across your gate to source remains zero. If they are in phase and have the same amplitude then they will cancel out. And that is what the feedback does actually.

So, it will look like a high pass filter. I mean your system will look like a low pass filter but if you look at PSRR it will look like a high pass filter for gate pole as dominant pole. Because at lower frequency you will get a rejection but at higher frequency you will not get the rejection. But when this non-dominant pole, this output capacitor kicks in then you have an additional pole and it will try to attenuate the signal. So, it will look like a band-pass kind of behavior. But if you make this output dominant then it will look like a perfect low-pass filter which is the desired case. But it's not easy to make the output pole as dominant because most of the cases the values of these output capacitors are very small.

So, there is no way unless you put an order of micro Farads or so. And we prefer on-chip regulators but on-chip mostly we can put 10s of Pico Farad. So, you can never make this output pole as dominant, that is the problem.

And that is one of the reasons sometimes at the output of switching regulator you need a linear regulator because switching regulators are noisy. They will have ripple in the output and you want to filter that. If you have a noise sensitive application, let's say RF or analog and it is driving very high current then you put a DC-DC converter followed by a linear regulator which we call as sub-regulator.

And if we keep the dropout very low then you will not lose too much in efficiency. And if your linear regulator has a very good bandwidth then you can filter out those ripples and output will be much cleaner. Instead of 10 mV, you might see less than 1 mV ripple in the output which will be sufficient to supply to your noise sensitive application.