Power Management Integrated Circuits
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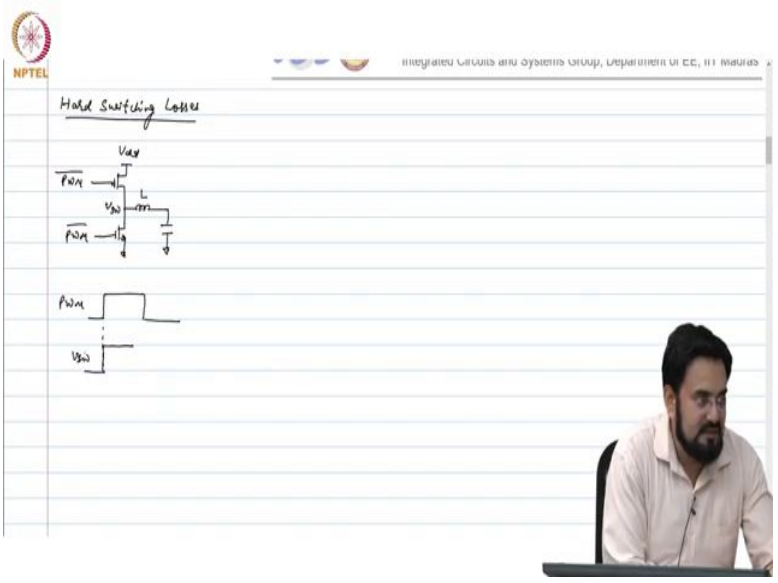
Lecture – 38
Hard Switching Loss in DC-DC Converters

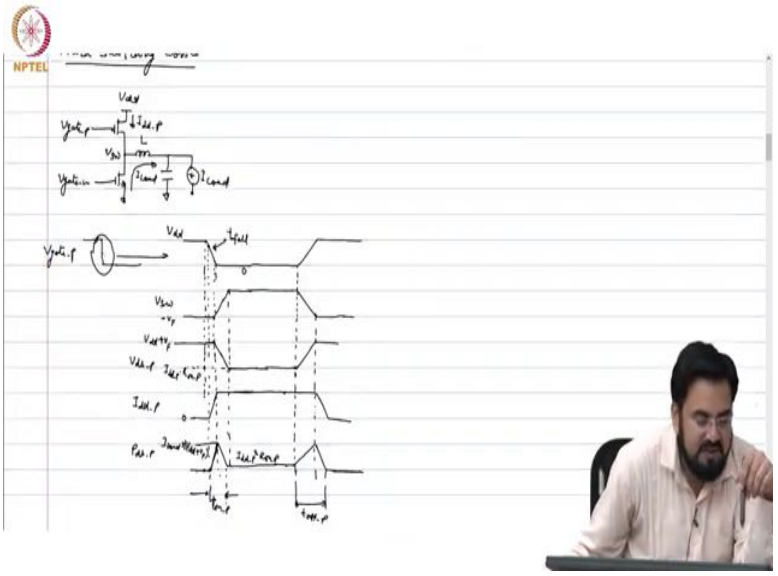


We had already talked about the gate driver switching losses and dead time switching losses. Gate driver switching losses does not depend on load current while dead time switching loss depends on load current and non-overlap time and switching frequency as well.

Dead time losses depend on how much percentage of one clock period we are spending into dead time. We always try to minimize the dead time in order to get better efficiency.

Hard Time Switching Losses: Hard time switching losses are also associated with the power FETs. The dominant component of loss will be due to the PMOS.

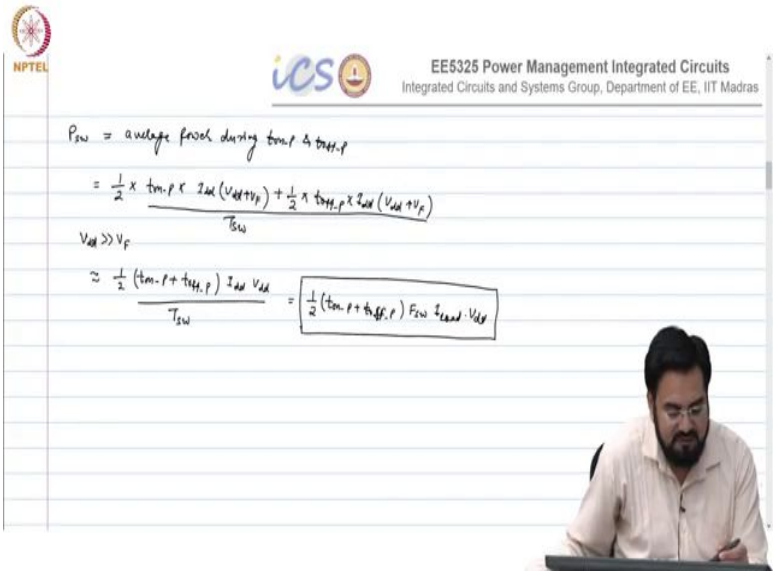
In the below figure, $V_{gate\text{-}p}$ and $V_{gate\text{-}n}$ have some finite rise time and fall time associated with them.



When $V_{gate\text{-}p}$ is going from supply voltage to zero voltage i.e PMOS is turning on, V_{SW} voltage will also start increasing. Initially, V_{SW} is at the $-V_F$(forward voltage of the diode) and will only start increasing when the body diode due to NMOS becomes reverse biased. So, which means as long as the diode is conducting, V_{SW} voltage will be maintained at $-V_F$. To reverse bias the body diode, PMOS has to supply the current and its $r_{ds\text{-}on}$ should be very low to do that and it will happen when $V_{gate\text{-}p}$ is closer to 0V. Waveforms of $V_{gate\text{-}p}$, V_{SW}, and $V_{ds\text{-}p}$ are shown in the above image.

$I_{ds\text{-}p}$ (current through PMOS) is initially zero and will start increasing when the difference between $V_{gate\text{-}p}$ and Vdd crosses V_{tp} and $I_{ds\text{-}p}$ will reach the maximum value when the voltage at $V_{gate\text{-}p}$ reaches 0V. Power across PMOS ($P_{ds\text{-}p}$) is the product of $I_{ds\text{-}p}$ and $V_{ds\text{-}p}$. Waveforms of $I_{ds\text{-}p}$ and $P_{ds\text{-}p}$ are shown in the above image.

When we are turning off the PMOS, V_{SW} will start decreasing and the load current will flow through PMOS until the body diode of NMOS becomes forward biased. $V_{ds\text{-}p}$ will increase when V_{SW} is decreasing and current through PMOS is not changing. So losses will be high during that time. Current will start flowing through the body diode of NMOS when PMOS completely turns off i.e voltage at $V_{gate\text{-}p}$ reaches Vdd.



Average power during t_{on-p} and t_{off-p} (t_{on-p} and t_{off-p} are labeled in P_{ds-p} waveform in the previous image) will be the Hard time switching losses(P_{SW}). Calculations for finding P_{SW} is shown in the above image.

$$P_{SW} = \frac{1}{2}(t_{on-p} + t_{off-p})F_{sw}I_{Load}V\,dd$$

We cannot ignore V_F always and if the value of Vdd is smaller and comparable to V_F then we have to consider the value of V_F in calculations. The value of t_{off-p} and t_{on-p} can be calculated from simulation and if we are using external fets then most of the time the datasheet will specify that. For a discrete power supply design, we use external fets. The value of t_{off-p} and t_{on-p} is higher for external fets compared to on-chip fets that's why Hard time switching loss is a dominant factor for discrete power supply.

For all the switching losses which are deadtime, gate driver, and Hard time, they will start dominating when F_{SW} is very high. Some of them are a function of load and some of them are not for example gate driver switching losses, but they all are functions of switching frequency. So, that is why most of the DC-DC converters or switching regulators we find in the market have a maximum switching frequency of around 10MHz, and the current would be less than 1A. But if we are looking at a 10 amp kind of current then we will see that achieving even 1 MHz is not easy with that because these losses are very dominant and they will kill your efficiency.