Power Management Integrated Circuits
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Lecture – 33
Volt-second Balance, Non-Idealities in the Power Stage of a Buck Converter

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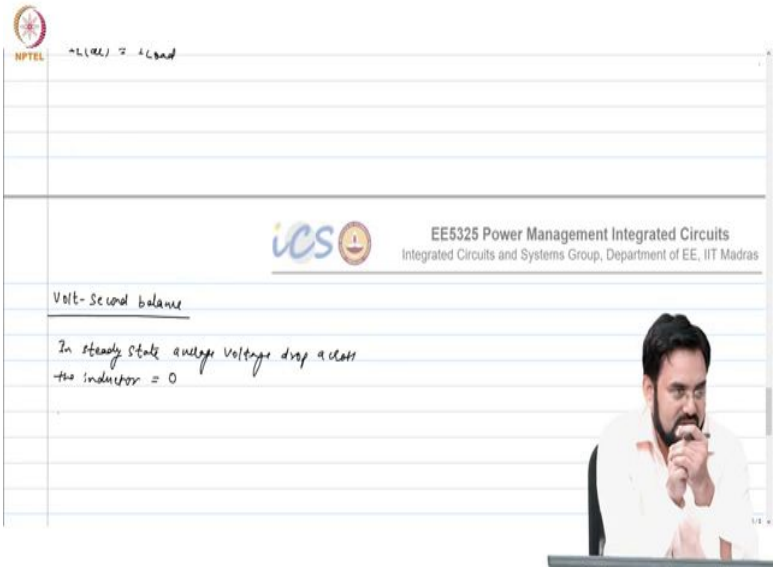

So there is something called volt-second balance. So, for this particular case, you already know that your output is D times V dd, but there might be some different architecture where you do not know the topology, ok. So, in order to find the relationship between V out and V in, that is what we use, volt-second balance, and irrespective of what kind of configuration you have in the power stage, you can always derive that, using that formula. So, let us see how it works. So, in steady-state, average voltage drop across, what should be the average voltage drop?

0, because it is a lossless component, and this is required to have a DC current because we know that my current will be an integrated voltage. So, if you apply any difference, it will keep integrating and current will never stop, it will keep rising. So, in order to have a current settled, the voltage must be maintained 0 across the inductor. Same, if we talk about the capacitor, then what has to be maintained, at 0?

The current has to be 0, otherwise your voltage will keep rising. So, they are exactly opposite to each other. Here current will rising if you give a, any voltage across the inductor, in case of capacitor, if you give a any current, positive or negative your voltage will never settle. So, in order to have in steady-state, you have to maintain the 0 voltage across the inductor and if you have to in steady-state for the capacitor you have to maintain the 0 current, average current.

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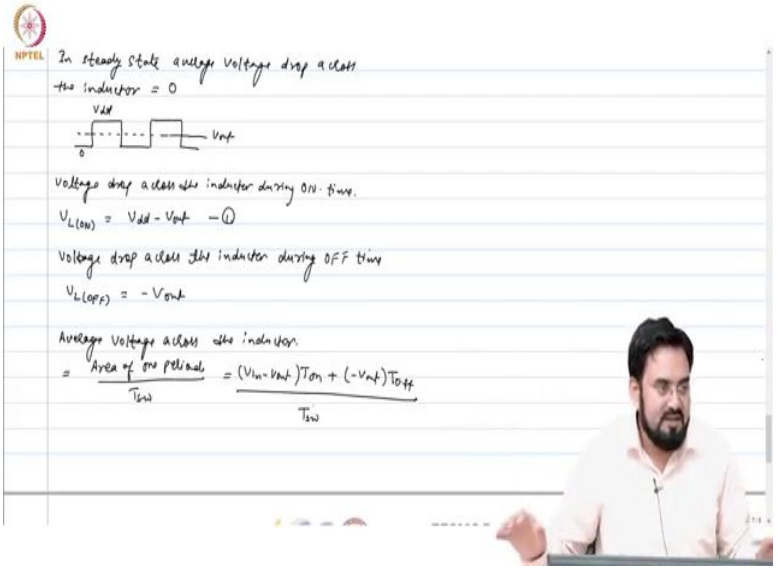

So, we know this is your PWM, 0 to V dd and average will be your V out. So, voltage drop across the inductor during ON time V_L equal to or let me say V_L, V _ L,on V dd minus V out; … during minus … V out. Average voltage across the inductor, what will be the average voltage?

Area of one period, it is a periodic signal divided by T sw, ok. So, what will be the area of? So, if you think this voltage across, you know this V in minus V out, V in minus V out and this is happening for T on times, plus during T off minus V out T off, divided by your period. Alternatively you can integrate, but you will get the same thing, which is integrate the square wave that is how you get. If you know the area, is straight forward, like a case of rectangle or triangle, you do not integrate, you just directly find the area and divide by time period and you get the average wave.

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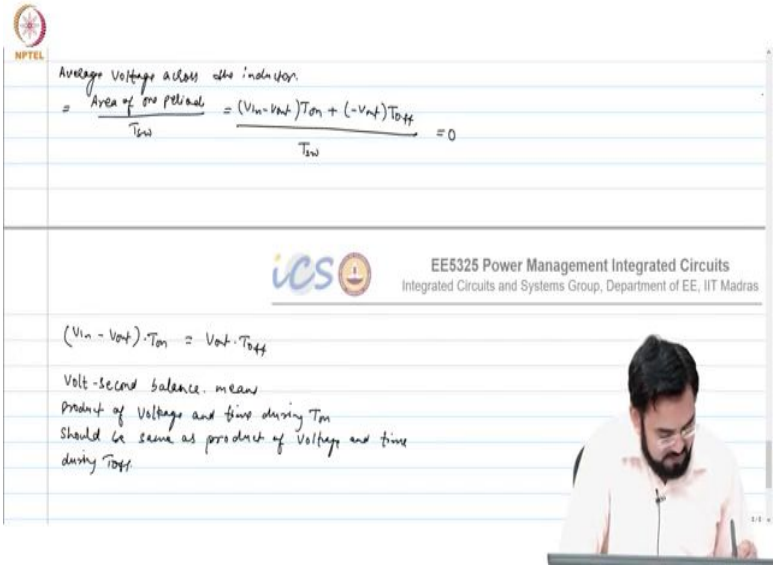

And this must be 0. So, can I say; V in minus V out T on equal to, into T off, correct. So, what does it mean? Which means in order to maintain the 0 average voltage across the inductor, the voltage during the on time should be same during the off time, ok. Basically, the voltage time, a voltage, product of voltage and time and that is why we call it volt second balance, means product of voltage and time during T on should be same as product of voltage and time during T off.

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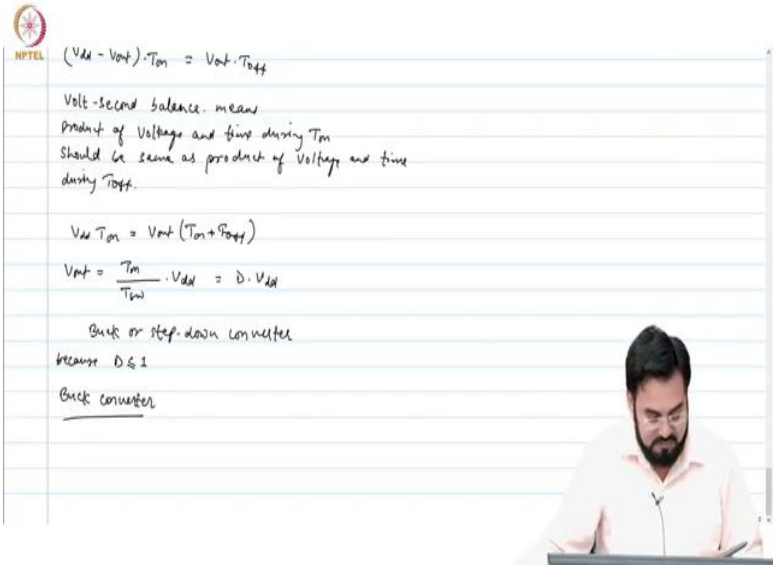

So, from here let us see. So, you have V in T on equal to V out T on plus T off. So, V out equal to, we defined it as V dd, sorry, let us call it V dd. So, V out equal to T on over, and T on plus T off is nothing but T sw into D times and this is nothing, but buck or step-down converter because D is always less than or equal to, maximum it can be 1, but if you have a load then there will be some drop in the power stage.

I mean, theoretically you say it is a lossless component, but practically it will have some losses because your windings will have some resistance, inductor windings. So, there is some finite resistance associated with, order of tens of milliohm or so, or depending upon what type of inductor you use, ok. So, it can only buck or step-down your output and that is why we call it buck converter, ok. When we will talk about the boost we will again do the same exercise and we will see what is the relationship between V in and V out.

The same concept you apply and you will get the relationship between V out and V dd or V out and V in. So, let us see how you implement the power stage here.

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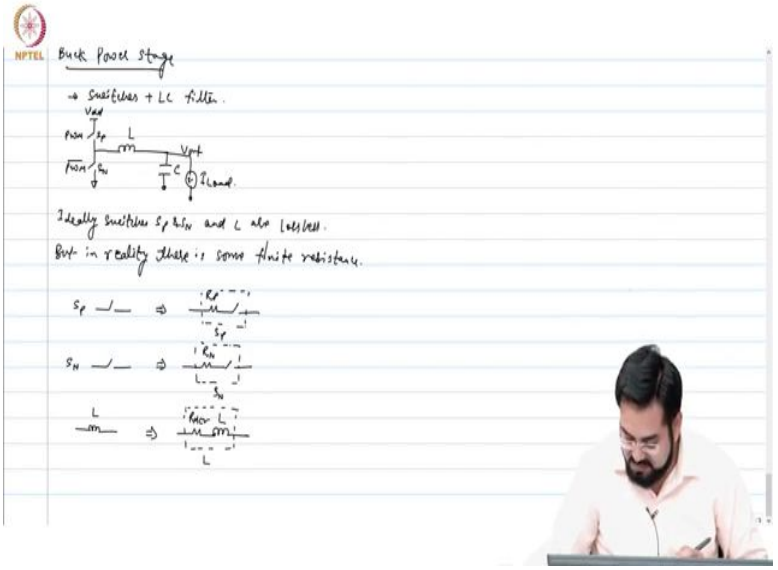

So, buck, so power stage means switches plus L C filter, ok. So, let us call it S_P and S_N, low side and this is driven by your, so, let us say I have a PWM signal, this is PWM and this is PWM bar. So, when PWM is high, switch S_P will turn on where inductor current will rise

and when S_N is on S_P is off, inductor current will fall with a slope of voltage across the inductor divided by L, and that is what will define your.

So, V out and if this has some load, so ideally switches S_P and S_N and L are lossless, ok. But in reality there is some finite resistance and that is what you have to model. So, let us say S_P you can model it with a switch and so I will call it R_P and this is your switch. S_N you model it R_N and this whole thing becomes your S_N and inductor you model it.

So, a lossless inductor with series R and we usually call it R dcr, DC resistance of the inductor. This is how you model, ok. Now, we will replace all the switches and inductor with this model and we will see what happens to the output.

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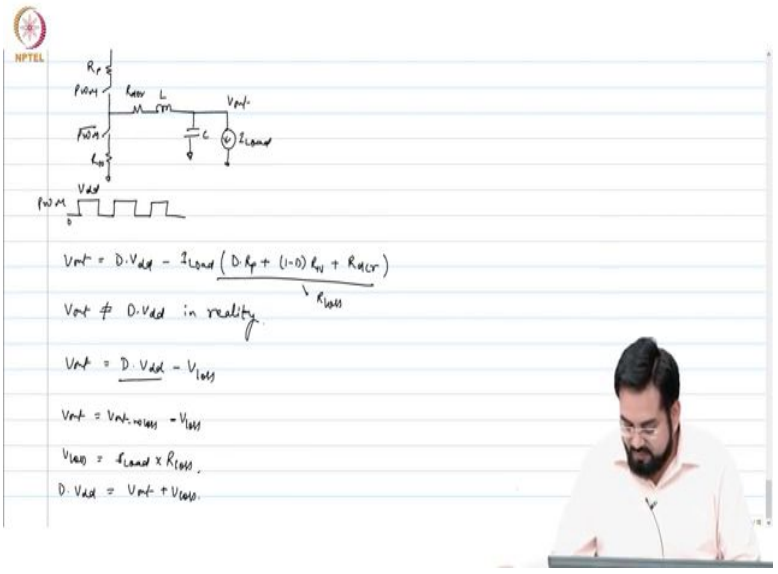

So, what will be the output? V out, this is your PWM signal. The duty cycle of D, D times V dd minus I load, into what?

So, during on time, the top switch is on, so the loss will be across your R P, so D times R P, then during off time. So, D times R P, sorry, yeah, correct. 1 minus D times R N and the current in the inductor is continuous, the current will flow during both on and off time, so it will be only R off, dcr, correct. So, which means V out is no longer D times V dd in reality. So, what do I do? So, if you know that V out is D times V dd, so let us say your V out is 5 volt. You want 2.5 volt output, you just feed a 50 percent duty cycle PWM signal at the input

and you will get a 2.5 volt output without any issue. But now it is no longer exact and this R P, R N and dcr are also unknown, you do not know what will be the resistance and even if you design it or pick the inductor for a particular value of these resistances.

Then, what would happen actually? Across temperature or due to tolerances those values may also change. So, you cannot even compensate for it, ok. So, can I call it; sorry. So, let us see V out equal to D times V dd minus V loss. So, we are losing some voltage there which I am simply calling V loss, ok. So, which means if this is your ideal V out equal to I will call it V out no loss, ok. V out no loss is nothing but D times V dd minus V loss.

So, and V loss is defined as, I_load into R loss, where R loss is nothing but this component. When you add everything together that is what is your. So, what do I need to do? If I want to achieve this, D times V dd is V out plus V loss, which means if I want to achieve the same voltage I have to increase the duty cycle, correct.

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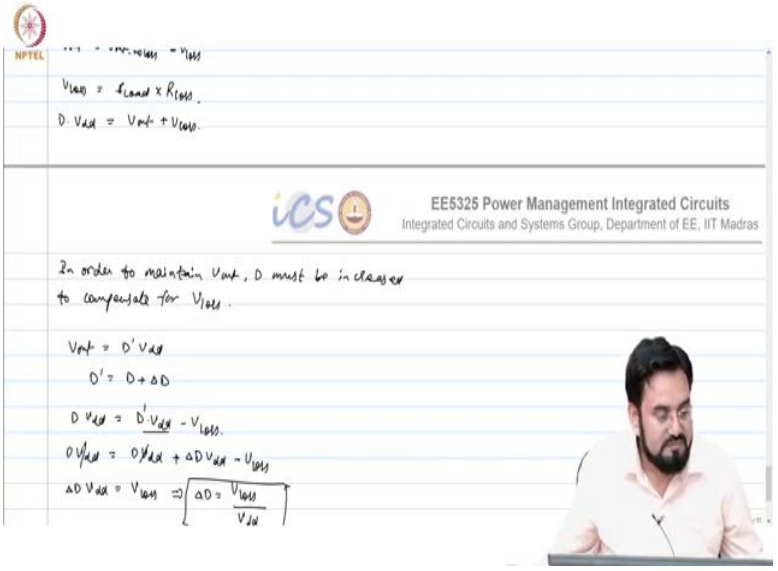

So, in order to maintain V out, D must be increased to compensate for V loss, ok. So, which means your V out is nothing but D dash I will call it, V dd, where D dash is D plus delta D, correct. And this is nothing but, D dash V dd is D times V dd minus V loss, or D V dd plus delta D, V dd equal to D V dd minus V loss. This cancels out.

So, let us fix this. This was plus that is all. So, delta D V dd equal to, this implies delta D equal to V loss over V dd, which means the change in duty cycle required is nothing but V loss over V dd ratio of, or V loss is nothing but delta D times V dd. So, if you know the V loss you can calculate how much duty cycle you need to change, in order to get the same output voltage. And V loss is nothing, but I_load into, so which means your V loss is a function of load current. So, this delta D also needs to be varied with the load current.

So, you can no longer operate this in the open loop. You have to do some calculation and change the duty cycle, and if you do it manually then it will be a very slow process. So, you use a feedback control here, the negative feedback and that is what negative feedback does, it varies your duty cycle based on changes in the R or load current in order to maintain the output voltage. And then you go back to again the negative feedback, compensation all the concept will apply here, because now in the loop you have LC filter and LC will you know, it is a complex filter. So, it will have a complex poles.

So, now, you have a double pole and a complex pole, if it is a very high Q, then at resonance you will get a 180 degree phase shift right away, so inherently it is a unstable system if you simply connect in the negative feedback. So, you need to stabilize it and we use to compensate it. So, there are different techniques to compensate it. But before that we will just look at different losses in the power stage. It is not the only loss, that R, there are switching losses also, there are magnetic losses. So, everything will contribute to your loss in efficiency.

And we will also take an example where we will see how it maintains the efficiency across wide range of V out over V in compared to LDO or linear regulator, where if dropout is increasing or V out by V dd is smaller, then your efficiency drops. And we will see how it is able to maintain around 90 percent or above across all the range. So, we will take 2 or 3 values and will see, calculate the efficiency, ok.