

Power Management Integrated Circuits
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Lecture - 26
Sources of Error in Linear and Switching Regulators

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The slide is titled "Sources of Error in Regulators" and lists the following items:

1. Loop Gain
2. V_{ref}
3. Mismatch in feedback resistor (error in β)
4. Offset

Below the list is a circuit diagram of a linear regulator. It features an operational amplifier (op-amp) configured as a voltage follower. The op-amp's non-inverting input is connected to a reference voltage V_{ref} . The op-amp's output is connected to the gate of a MOSFET. The MOSFET's source is connected to ground, and its drain is connected to the output node. A feedback resistor R_1 is connected between the output node and the op-amp's inverting input. Another resistor R_2 is connected between the output node and ground. The output voltage is labeled V_{out} .

An inset in the bottom right corner shows a man with a beard and glasses, wearing a light blue shirt, speaking into a microphone.

Sources of Error in Regulators: so, even though I will be talking in perspective with linear regulator, but all these sources of error are applicable for switching regulator as well.

So, loop gain, offset I will that is one source one of the sources of error, but I will put that at the end. Before that I want to just cover the simple sources. So, we know V_{ref} , so if you have any error in the reference that will directly get affected at the output. Then mismatch in feedback resistor, correct, that will be error in your beta. Offset, ok.

So, now, for this particular, we are not looking for any stability or AC analysis, so I will just draw a very simple regulator R_1 , R_2 .

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4. Offset

$A_0 = A_{01} - A_{02}$

Closed loop gain
 $= \frac{A_0}{1 + \beta A_0} \approx \frac{1}{\beta} \text{ if } \beta A_0 \gg 1$

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So, what is your V_{out} ? In terms of V_{ref} .

V_{ref} over beta. But it is really not beta actually, when you say beta you consider A_{nought} equal to infinity. So, in reality your gain is, so closed loop gain equal to, ok. So, if you and this is if beta A_{nought} is much much larger than 1, and that is why we make it independent of open loop gain, correct or A_{nought} . But this is not true in reality, your A_{nought} is infinite, ok.

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The slide features a header with the ICS logo, the text "EE5325 Power Management Integrated Circuits", and the NPTEL logo. Below the header, handwritten calculations are shown on a grid background. A video inset in the bottom right corner shows a man with a beard and glasses, wearing a light blue shirt, speaking.

Example :
if $\beta = \frac{1}{2}$
 $V_{ref} = 0.6 \text{ V}$
 $V_o = 1.2 \text{ V}$

$$V_o = \frac{A_o}{1 + \beta A_o} V_{ref}$$

assume $A_o = 100$

$$V_o = \frac{100 \times 0.6}{1 + 50} = \frac{60}{51} = 1.176$$
$$Error = -0.023 \text{ V} \approx 2\%$$

So, if example, if let us say beta equal to half, your V_{ref} equal to let us say 0.6 volt. So, V_{out} we know we are expecting 1.2 volt, ok. But if we go from that equation V_{out} equal to A_{nought} over $1 + \beta A_{nought}$ V_{ref} and assume A_{nought} equal to 100. Now, your V_{out} will become 100 over $1 +$, how much is that? 50.

So, 1.76 roughly, that is 1.176.

Minus. So, error is how much? Minus 0.023 volt which is close to 2 percent, correct. So, we have introduced 1 percent. So, if you look at the gain A_{nought} 100, ok, so if beta is 1, 100 will, gain of 100 will correspond to almost 1 percent error, but since beta is amplifying your output. So, 1 percent becomes your 2 percent.

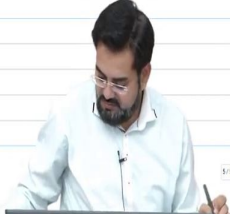
So, if your beta is let us say even smaller, then your error will be larger in that case because your loop gain will product of beta into A_{nought} will further reduce, ok.

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Handwritten notes on a whiteboard:

if $\beta = \frac{1}{2}$
 $V_{ref} = 0.6 \text{ V}$
 $V_o = 1.2 \text{ V}$
 $V_o = \frac{A_o}{1 + \beta A_o} V_{ref}$
assume $A_o = 100$
 $V_o = \frac{100 \times 0.6}{1 + 50} = \frac{60}{51} = 1.176$
Error $= -0.023 \text{ V} \approx 2\%$
In order to reduce error, we should
have large βA_o or for smaller β
 A_o must be increased ($> 60 \text{ dB}$)
B) V_{ref}
 $V_o \approx \frac{V_{ref}}{\beta}$



So, which means, in order to reduce error we should have large beta A nought, or for smaller beta, A nought must be increased, usually more than 60 dB or so. So, if you have a 60, your A nought is 60 dB which is your 1000, so 0.1 percent error in feedback voltage which means 0.2 percent error in the output voltage.

So, 0.2 percent is not that large, as usually if you are let us say less than 1 percent then it is acceptable, but you have to make sure your overall error, overall error I mean, including your line regulation, your load regulation and error in the V ref everything will remains within your specification, ok. Whatever error is basically specified for that particular voltage; if it remains within that then it will be acceptable, ok.

And that is why we try to improve on each and every thing, so that you minimize the error, so that you can get more room for other errors or for your transient response because we know it is going to undershoot or overshoot during transient. So, if you remain very close to your steady state voltage, desired steady state voltage then you get more room for your line and load transient, ok.

So, we cannot afford, so, if your regulation limit is plus minus 5 percent that does not mean that you can afford to have a 5 percent error because you are line transient and load transient will make it to go beyond 5 percent and it will go out of regulation, ok.

Second is your V ref. So, we know V out is, V ref over beta. So, any error in V ref will directly affect your V out, ok.

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any error in Vref will directly affect your Vout.
Error is more for smaller β .

② Mismatch in feedback resistors.

$$\beta = \frac{R_2}{R_1 + R_2}$$

$$V_{out} = \frac{V_{ref}}{\beta}$$

Assume, R_2 & R_1 have $\pm \Delta R$ error.

$$R_2 \rightarrow R_2 + \Delta R$$

$$R_1 \rightarrow R_1 - \Delta R$$

$$\beta' = \frac{R_2 + \Delta R}{R_1 - \Delta R} = \frac{R_2}{R_1 + R_2} \left(1 + \frac{\Delta R}{R_2} \right)$$

So, if your beta is smaller, then again smaller error in V ref will get amplified. So, error is more for smaller beta, correct; again the same thing which we looked at the loop gain. So, if we have a 1 percent error in the V ref; that means, you have a 1 percent error in your feedback voltage and now when you are looking at the output that is amplified by your 1 over beta factor. So, if it is a 2, then it will become 2 percent error in the output. So, that is why having a smaller V ref is not very good in terms of error.

So, let us say you want 1.2 volt output, so one way like you have a V ref 1.2 volt and have a beta 1. Another way is have a V ref 0.6 volt and have a beta 2. So, having a beta 1 may have a lesser error compared to having beta 2 or V ref 1.2 volt will give you lesser error compared to 0.6 volt, ok.

Then third is your mismatch. So, your beta is R 2 over R 1 plus R 2 and we know V out is V ref over beta. So, assume R 2 and R 1 have plus minus delta R error. I am assuming same error. It may be different also, but this is for simplicity. So, what will be the worst case? Both will have plus delta, or one will have plus delta and other will have minus delta?

Different, because if both have a same then it will cancel out. So, there will no error as such. If both are moving in the same direction, so that ratio will not change as such, ok. So, R_2 becomes $R_2 + \Delta R$ and R_1 becomes $R_1 - \Delta R$. So now, your beta will become $R_2 + \Delta R$ and plus minus delta will cancel out, so this will remain $R_1 + R_2$. And I can say that, so your beta, I will say beta dash, ok. $1 +$, which I can say this is your beta $1 +$, I can call it delta beta. So, your beta is increased by a factor of delta beta or delta R by R_2 .

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if error in ref value directly affect your V_{out} .
Error is more for smaller β .

⑤ Mismatch in feedback resistors.

$$\beta = \frac{R_2}{R_1 + R_2}$$

$$V_{out} = \frac{V_{ref}}{\beta}$$

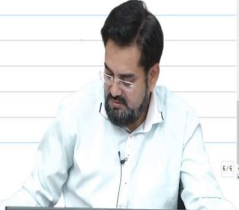
Assume, R_2 & R_1 have $\pm \Delta R$ error.

$$R_2 \rightarrow R_2 + \Delta R$$

$$R_1 \rightarrow R_1 - \Delta R$$

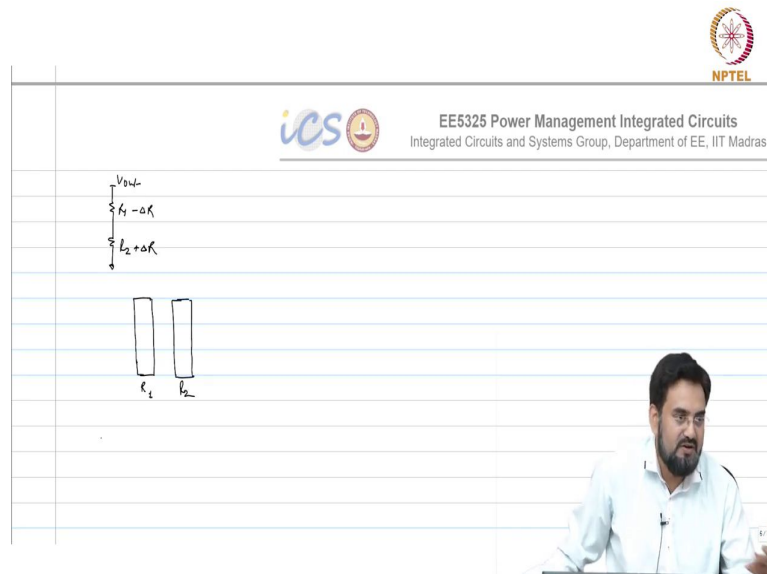
$$\beta' = \frac{R_2 + \Delta R}{R_1 - \Delta R} = \frac{R_2}{R_1 + R_2} \left(1 + \frac{\Delta R}{R_2} \right)$$

$$= \beta (1 + \Delta \beta)$$

$$V_o = \frac{V_{ref}}{\beta'}$$


So, if this has again R_2 has let us say one percent error and R_1 has a minus 1 percent, then beta, your beta will be increased by 1 percent, ok. And we know that V_{out} is, so now, V_{out} will become V_{ref} over beta dash and that will have same amount of error, ok. And where does it come from, that mismatch?

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So, this is your feedback resistor. So, this is your V_{out} , R_1 , R_2 . So, so what happens when you layout them in the chip? Ok. So, so if this is your R_1 , this is your R_2 . So, what happens; this when you place the basically conditions at that particular location may be different then what is seen by the other resistor, ok.

One thing might be like your, due to the process you have some mismatch and that may come due to the error in the basically non-ideal effects in your process. So, one may have a slightly smaller width or length compared to the other that will come from process itself, that is a one thing. Other thing is your temperature gradient. So, this might see a different temperature compared to the other, even though it may be a very small, but you have to consider that depending upon how much it is affecting, even if it is a 0.1 percent it will have some effect on your output, ok. So, 0.1 percent error it is being introduced in your output.

So, we try to match them and we apply some layout techniques to make sure they are matched and just like common centroid. And so, what we do? We split them in pieces instead of having a single R_1 , single R_2 , we split them in pieces and distribute equally, so that on an average the total resistance is seeing the same effect and they will cancel out. So, error is averaged out and becomes close to zero, ok.

So, we will talk about the layout techniques for matching. And this is applied in not only in resistors, but in your amplifier you need to match the input pairs, diff pair because if g_m 's are different then it will again introduce the error or offset in the output, or you will have a input referred offset, it will get translated into error in the output. So, those offsets and everything is reduced.

So, first thing we precautionary, we try to reduce the error as much as possible by design and by layout, ok. So, when I say design basically by properly choosing the transistor sizes and how you split them, instead of using a two single big transistor we split them in multiple transistor and distribute them in the layout, so that error is averaged out, and same thing we apply with the capacitor and resistor the same concept.

So, common centroid is the one technique, then inter digitized. Inter digitize means you inter leave the, so let us say I break them in 4 pieces R_1 and R_2 . So, put one piece of R_1 , then adjacent to that R_2 , $R_1 R_2$, $R_1 R_2$ just like you inter leave them. So, the error will be averaged out in that case. So, we try to place them as close as possible, that is a one thing. So, that if you put one guy here and other is like 100 micron away, then they will the difference will be much larger in all the conditions whatever is seen by each resistor.

So, we will talk about those layout technique later, but that is the one way and then after that if you are still not meeting your accuracy requirement then we use some techniques in the design itself like offset cancellation to reduce that or completely cancel the offset, bring it to almost zero actually, ok. So, it all depends on what kind of accuracy you are looking for, especially for these regulators and all those you may not require offset cancellation quite often if you have taken care in design and layout.

But think about ADCs, like 10 bit, 12 bit ADCs they require accuracy of like 100s of microvolt or so. So, there you may cannot afford to have any offset. So, there you have to cancel offset there is no other way because achieving those kind of accuracy with layout, it is not possible. Just by layout you cannot cancel everything.