Power Management Integrated Circuits
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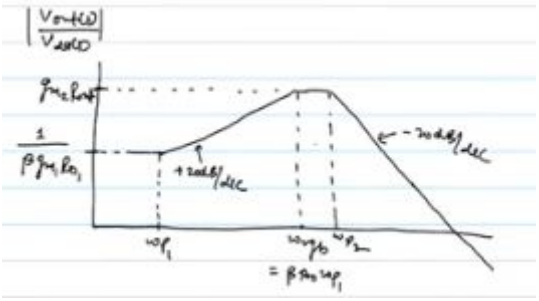
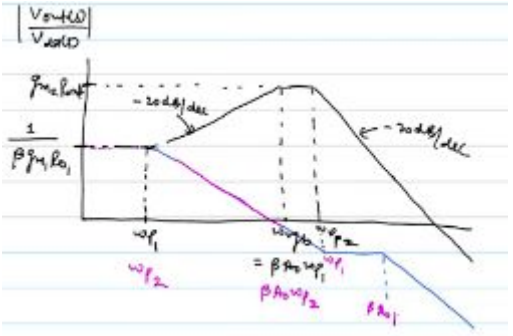
Lecture – 25
PSRR of PMOS versus PSRR of NMOS LDO

- Magnitude plot of the PSRR of the PMOS LDO when the error amplifier pole ω_{p1} is dominant:



  - Around ω_{ugb}, the impedance of capacitor C_{o1} is very small and the gate of the PMOS pass element gets short-circuited to ground. This means that the output stage of the PMOS LDO becomes a common gate amplifier at frequencies around ω_{ugb}, so the PSRR v_{out}/v_{dd} becomes $g_{m2}R_{out}$.

- Magnitude plot of the PSRR of the PMOS LDO when the output pole ω_{p2} is dominant (pink and blue curve):



  - The PSRR stays flat (at the line regulation) at frequencies $\omega < \beta A_0 \omega_{p2}$, i.e. at frequencies $\omega < \omega_u$.
  - The zero at ω_{p1} cancels with the non-dominant error amplifier pole ω_{p1}.
  - Thus, when the output pole is dominant, the PSRR is always non-increasing, i.e. it never increases beyond the line regulation (whereas the PSRR degrades at frequencies near ω_{ugb} when the error amplifier pole is dominant).

    - When the output pole is dominant, the response to both line and load transients is better than when the error amplifier pole is dominant.

- There are two paths from V_{dd} to V_{out} in a PMOS LDO (one through the transconductance g_m and the other through r_{ds}) but there is only one path (through r_{ds}) in an NMOS LDO. Thus, the line regulation and PSRR of an NMOS LDO is better than that of a PMOS LDO.
- The line regulation of the PMOS LDO is $1/(\beta g_{m1} R_{o1})$ whereas the line regulation of an NMOS LDO is $1/(\beta g_{m1} R_{o1} g_{m2} r_{ds})$, i.e. it is further reduced by the factor $g_{m2} r_{ds}$.

- The general shape of the PSRR magnitude curves of the NMOS LDO is similar to the respective curves of the PMOS LDO in both cases (error amplifier pole dominant and output pole dominant).
- The NMOS LDO has a faster response to line transients than the PMOS LDO since it has a better (smaller) PSRR. However, the gate voltage of an NMOS LDO needs to be boosted beyond the input voltage if the dropout voltage is to be low (smaller than the threshold voltage).

- A good (i.e. small) PSRR is important when an LDO is used as a sub-regulator in cascade with a switching regulator. The LDO would need to have a sufficiently high rejection (i.e. a sufficiently low PSRR) at the switching frequency of the switching converter to filter out the ripples at that frequency.