Power Management Integrated Circuits
Dr. Qadeer Ahmad Khan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 22
Effect of RHP zero on Stability,
Mitigating the Effect of RHP zero,
LDO with NMOS Pass Element

- The loop gain magnitude plot shifts upwards as the feedback factor β increases while the loop gain phase plot does not shift. This means that the unity loop-gain frequency shifts to the right (i.e. increases) as β increases. Thus, the worst (smallest) phase margin occurs for β = 1 (unity feedback), assuming that the maximum value of the feedback factor β is 1. So, if the loop is compensated for β = 1 (i.e. the loop is unity gain compensated) then it will remain compensated (with a better phase margin) for all other values of β (since β □ 1).

- Miller compensation introduces a right half-plane zero (RHP zero) which contributes negative phase (or phase lag).
- The negative phase contribution of the RHP zero reduces the phase lag that can be contributed by the non-dominant pole at the unity loop gain frequency, for a given phase margin.
- The negative phase contribution of the RHP zero is - $\tan^{-1}(g_{m2} / g_{m3})$ and can be reduced by ensuring that $g_{m2} << g_{m3}$. This is difficult to ensure at light load, when g_{m3} is much smaller than at higher load currents. Thus, one looks for ways to mitigate the effect of the RHP zero.
- There are three ways to mitigate the effect of the RHP zero.
    - Insert a nulling resistor in series with the Miller capacitor. This either cancels the RHP zero or converts it into an LHP zero which contributes phase lead.
    - Design to ensure that $g_{m2} << g_{m3}$.
    - Insert a buffer (can be a source follower) instead of the nulling resistor, to block the forward path through the Miller capacitor.
        - The RHP zero occurred due to two alternative forward paths - one through the transconductor and the other through the Miller capacitor. The RHP zero is avoided by eliminating one of the forward paths. The feedback path (through the buffer) ensures the Miller effect.
        - The source follower buffer introduces an additional pole and an LHP zero at $(g_m + g_{ds})/C$.
        - When the unity-gain buffer is replaced by an amplifier of gain 'A', the Miller effect is enhanced (i.e. the Miller multiplication factor increases by 'A') and the dominant pole is pushed further to the left. The size of the compensation capacitor required is further reduced by the factor 'A'. This variant of Miller compensation is known as Ahuja compensation.

- Miller compensation places the dominant pole at the output of the first stage (or the error amplifier). If the output pole is to be made dominant, the pole at the output of the error amplifier needs to be pushed to a higher frequency. This can be done in two ways.
    - Reduce the impedance (w.r.t. ground) seen at the output of the error amplifier. This can be done by inserting a buffer, due to which the impedance seen at the output of the first stage (or error amplifier) is $\cong 1/g_m$.
    - Reduce the capacitance seen at the output of the error amplifier. This can be done by using an NMOS transistor as the pass element instead of a PMOS transistor. The NMOS device is bound to be smaller than a PMOS device for the same transconductance g_m since it has a higher mobility, so its gate capacitance would be smaller.
        - Using an LDO with an NMOS pass element would turn the output stage of the LDO into a source follower whose gain is approximately unity. Hence, all the loop gain would have to come from the error amplifier (which would need to have two or more stages).
        - An NMOS LDO would need to have a high dropout voltage (greater than the threshold voltage of the NMOS device) so that the gate voltage can remain lower than the drain voltage (V_{in}) while keeping it in saturation. Otherwise, the gate voltage would have to be boosted beyond V_{in} if the dropout voltage is to be small. This can be done by using a separate supply voltage (larger than V_{in}) for the error amplifier - if only a single supply voltage is available, then capacitive charge pumps can be used to boost the supply voltage.
        - Since the output stage of an NMOS LDO is a source follower, the impedance seen at the output node is $1/g_m$, so the capacitance at the output node needs to be quite large to make the output pole dominant. This is useful when the LDO has to drive a very large output capacitor.
        - An NMOS LDO has a better PSRR than a PMOS LDO.