Power Management Integrated Circuits
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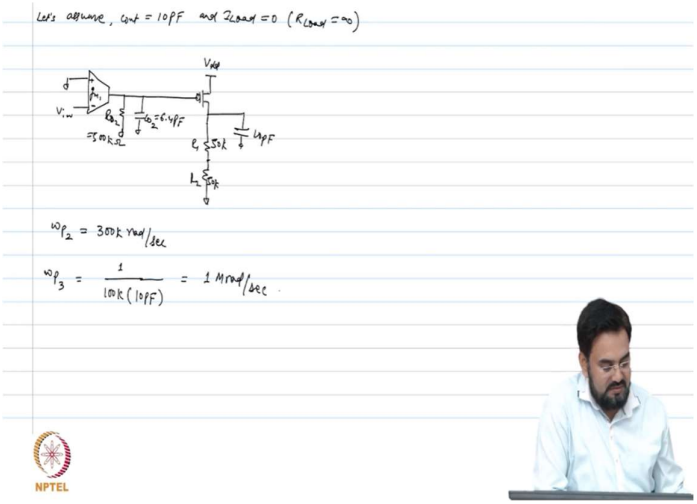
Lecture- 19
Dominant Pole Compensation at No-Load

In previous lecture we looked at how we find the value of your compensation cap for Dominant Pole Compensation. We continue with that and we will just consider one more example.

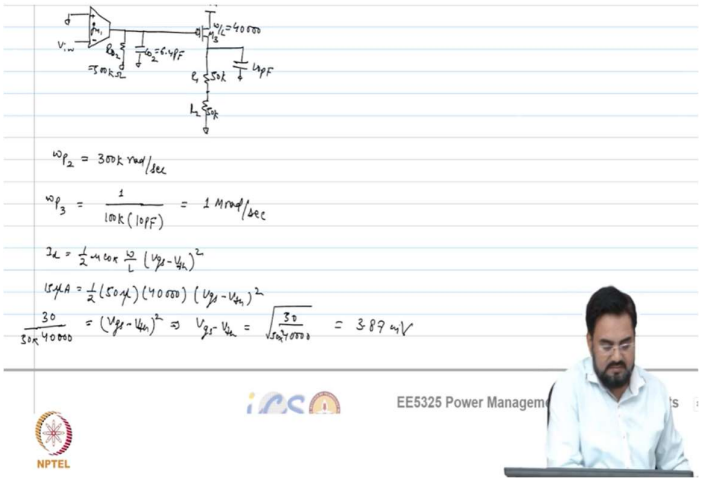
Let's assume your C_{out} =10 pF and I_{load} = 0. I_{load} = 0 means $R_{load} = \infty$. The circuit diagram is shown in below figure.



I am just assuming feedback factor(β) is 0.5 and choosing feedback resistors as 50 kΩ each. If I want 1.5 V output voltage then V_{ref} should be 0.75 V.

So, one thing you need to remember if you change the load then it will change your output resistance and your output pole will get affected. So, C_{out} =10 pF and R_{out} =100 kΩ, so we will get ω_{p3} at 1 Mrad/sec.

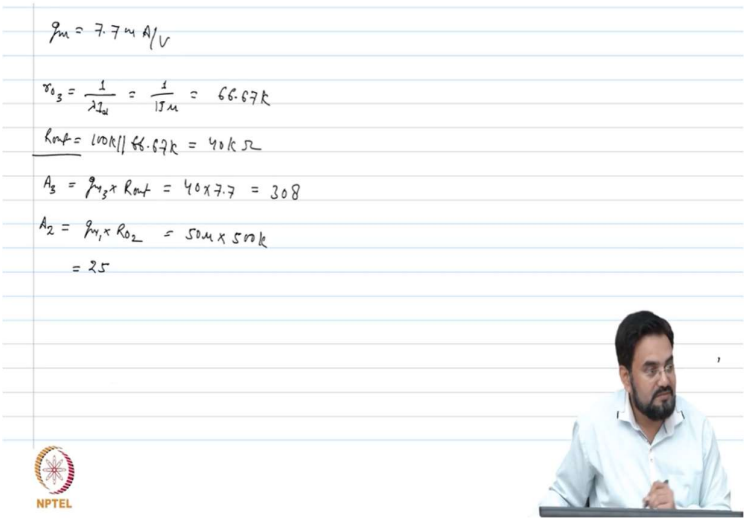
To supply maximum current of 10 mA by this pass element, we got the ratio $\frac{W}{L}$ = 40,000. At no load I_D = 15 μA and at this current the overdrive voltage is 3.8 mV as shown in below figure.



So, $g_{m3} = \frac{2I_D}{V_{ov}} = \frac{2 \times 15\mu}{3.87m} = 7.7$ mS

Student: Sir, while calculating ω_{p3} we forgot to consider the output resistance of MOSFET in R_{out}.

Ok. Since pass element is a minimum channel length device, so if I consider channel length modulation (λ) is approximately 1, then $r_{o3} = \frac{1}{\lambda I_D} = \frac{1}{15\,\mu} = 66.67$ kΩ. After considering this we will get $R_{out} = 40$ kΩ. So, $C_{out} = 10$ pF and $R_{out} = 40$ kΩ gives ω_{p3} as 2.5 Mrad/sec.

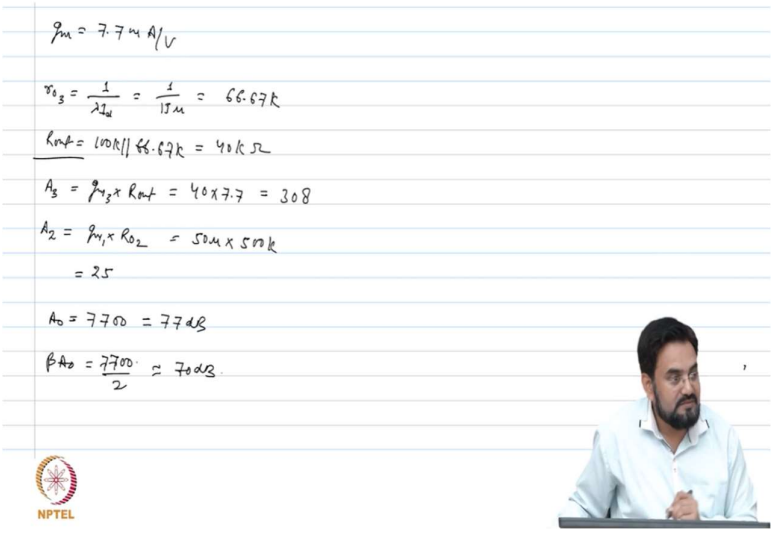


A_2 = gain of your first stage (Dc gain of op-amp)

A_3 = gain of your second stage

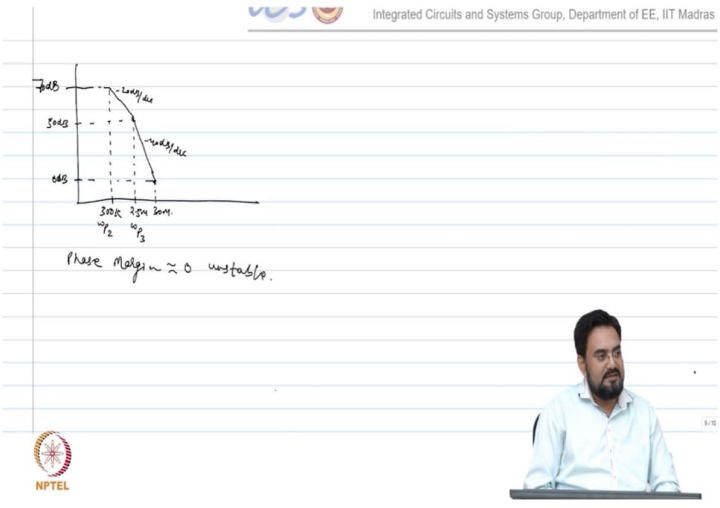
So, first stage gain is low and output stage gain is higher because pass element g_m is very large and R_{out} is also very large. And if you calculate the same output stage gain at 10 mA you will see that it will drop actually.

So, overall gain is 25 x 308 = 7700 = 77 dB



And If you consider the feedback factor(β) then it will further drop by 6 dB. So, loop gain (Aβ) is 7700 x 0.5 = 3850 which is close to 70 dB.

The bode plot for loop gain is shown in below figure.



Note that exact ω_{ugb} we will get as 44.5 Mrad/sec. And the phase at ω_{ugb} is almost 180° because both poles will have a 90° phase contribution at ω_{ugb}. So, phase margin is 0° which implies that system is unstable.

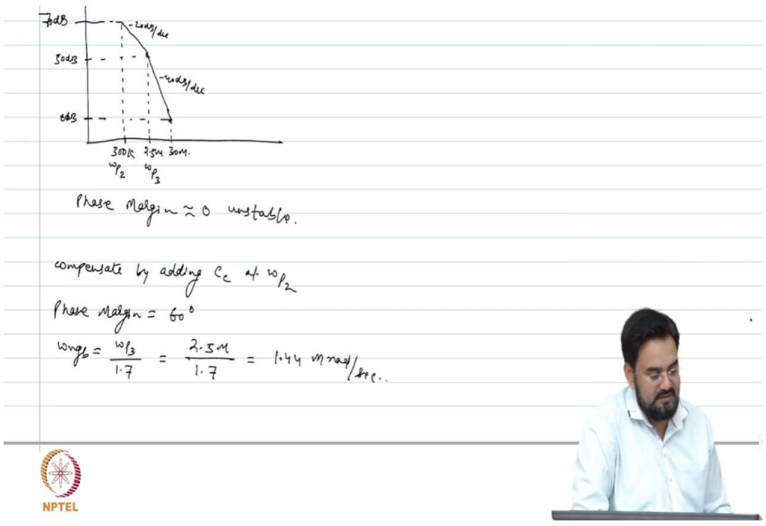
If I want to compensate it, shall I add the capacitor at output or at ω_{p2}?

Student: At ω_{p2} because to compensate at ω_{p3} we will require a very large cap.

Yeah, when you compensate at the output, your worst case will be the maximum load because at the maximum load your R_{out} will be very low. So, you require a very large cap to make it dominate. But if you put the cap at ω_{p2}, then your worst case is the light load because at the light load your output pole will be at lower frequency.

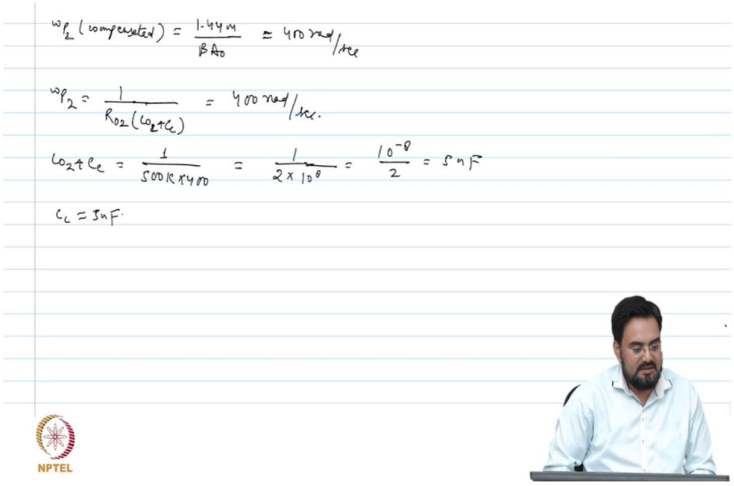
So, if your dominant pole is at ω_{p2}, then as you increase the load your second pole will be pushing at higher frequency and it will further improve your phase margin. So, if you compensate at a light load by putting the compensation cap at ω_{p2}, then for higher load it will be automatically compensated because your second pole will be moving at higher frequency. And that is what you want. You want to move your non-dominant pole outside your ω_{ugb}.

So, I want to push this ω_{p3} outside your ω_{ugb}, which means ω_{p2} has to be reduced. And to get 60° phase margin your non-dominant pole should be roughly 1.7 times of your ω_{ugb}.



DC loop gain (Aβ) is 70 dB which is roughly 3500.

So, ω_{p2} after compensation is at 400 rad/sec. To place ω_{p2} at 400 rad/sec the compensating cap (C_C) required is 5 nF and the calculations is shown in below figure.



This 5 nF is again a very large cap and it is almost impossible to put on-chip. You can put, but then all the area will be occupied by your capacitor compared to your circuit areas ok, 90% area will be taken by your capacitor which is not preferable.

Which means if you want to do the dominant pole compensation, you will again require very large cap, whether you put it at the second stage or at first stage. Obviously, at the second stage it will require even larger which is only possible with the external cap like order of microfarad. 5 nF is possible to put on-chip, but again it will take a lot of area. So, practically it is not feasible, and we never put order of nanofarad of cap on-chip until unless you are only designing the regulator chip. But most of these regulators are part of a bigger system, and you do not want to bloat the area just by increasing the size of your regulator.

So, 5 nF is quite large to implement on-chip. So, we look for alternate way of reducing the cap size. So, we require miller compensation.