Power Management Integrated Circuits
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Lecture - 18
Dominant Pole Frequency Compensation

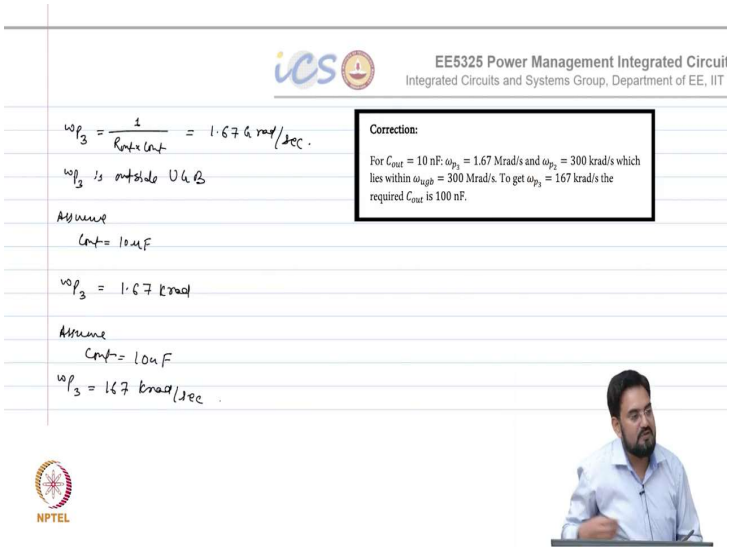
Now, if you assume the gain of first stage as 40 dB and second stage maybe 20 dB or so. So, with the 60 dB if you start and this ω_{p2}= 300 Krad/sec is the low frequency pole.

If you start with 60 dB DC gain, so after 3 decades, which means your ω_{ugb} will fall at 300 Mrad/sec. So, both the other poles are outside your ω_{ugb}. So, you may not need to compensate with this C_{out}.

Now, assume $C_{out} = 100$ µF then ω_{p3}= 167 rad/sec. Now this will become as dominant pole. And if you start with again 60 dB then ω_{ugb} will fall at 167 Krad/sec. We know that ω_{p2}= 300 Krad/sec and it will fall outside your ω_{ugb}. So, again you may not need to compensate.

Which means if you use a very large C_{out} or very small C_{out}, you may not require a compensation because it will behave like a first order system.

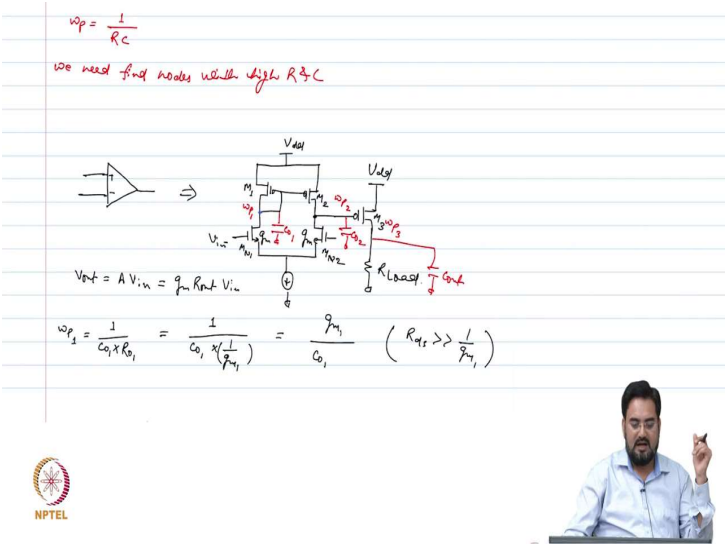
Now, I assume $C_{out} = 100$ nF then ω_{p3}= 167 Krad/sec and we know that ω_{p2}= 300 Krad/sec. Now both the poles are pretty close to each other and you have a second order system which needs to be compensated.



So, if you are designing for a very low C_{out} then for this particular load current of 10 mA you may not have to compensate. But the problem here is your load can be zero also.

So, both the cases you have to consider. There could be a case where your system is drawing a fixed load. Let's say it is on-off system, which means it is either drawing a no load or full load. In that case if the system is turned off, you do not need to regulate the supply at all. When the system is turning on, then it will draw this 10 mA current. So, in this case whether you require a compensation or not it will be determined by the value of C_{out}.

But let's say your load is variable from 0 to 10 mA.



Zero load means your R_{load} will become infinite. So, the current which will flow into the pass element will be only the current through the feedback resistor. You have another R-arm which is not shown in above figure. We use R-arm for feedback factor(β) and usually that resistance is very large. Both the resistance may be like minimum of 100KΩ. Even if you choose 50KΩ each, they are in series and output voltage is 1.5 V. So, 15 µA current is flowing.

With this 15 µA current, you have to determine what will be the R_{out} and this R_{out} will be very large. So, even with C_{out} = 10 pF you might see your pole might fall within your ω_{ugb} and you may have to compensate at light load. Since we are designing the LDO to cater to all the load variations from 0 to 10 mA, so we have to consider the worst case.

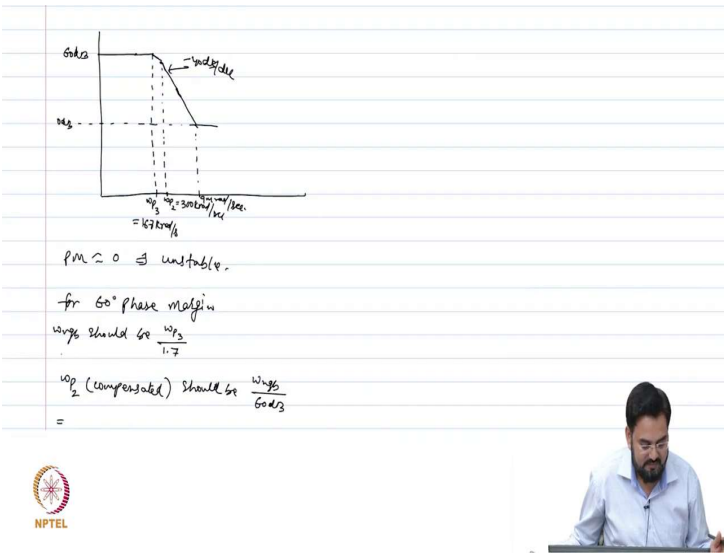
So, here the worst case will be the zero load current. If you compensate it for zero load current, then it will be automatically compensated for higher current because at higher current the output pole will be moving further at higher frequency. And if you are designing for a fixed load, then the worst case will be the midrange C_{out}.

That's why you cannot consider a fixed cap or fixed load while designing an LDO. Always consider the worst case. And the worst case is when both the poles ω_{p2} and ω_{p3} fall within your ω_{ugb}. And mostly when they are falling within ω_{ugb}, the worst ever case will be when both are very close to each other.

So, there is something called capless LDO, where on the output you do not put intentionally any cap, it's only the parasitic cap and it is order of picoFarad. In that case, you have to compensate it for the lightest load which is order of micro amps.

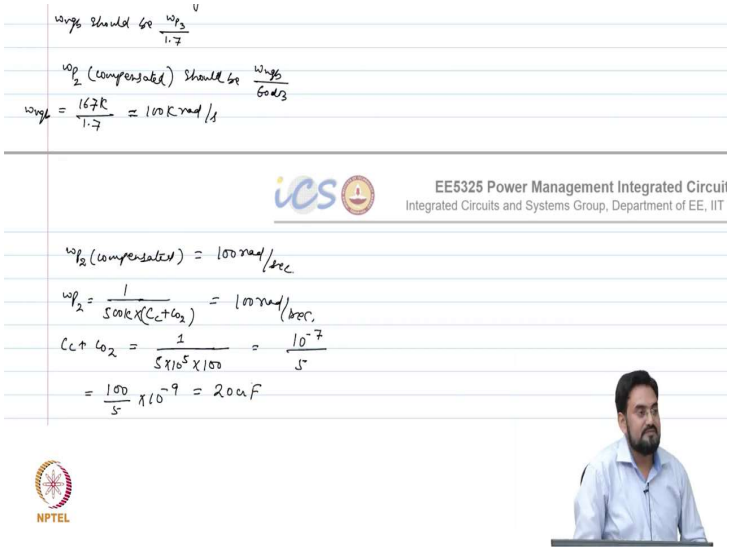
Now, if I want to design for C_{out} of 100 nF case and 10 mA, how are we going to compensate? Since C_{out} is fixed to 100 nF, the only choice you have is to add the capacitor at ω_{p2}. I mean if you already had a very high cap then it is self-compensated. When I choose C_{out} of 100 µF, then it is self-compensated because the second pole is outside your ω_{ugb}. You require a compensation only when your C_{out} is falling within range of 100 nF or so.

So, for this case ($C_{out} = 100$ nF), the bode plot is shown in below figure. Note that exact ω_{ugb} we will get at 5.3 Mrad/sec. And the phase at ω_{ugb} is almost 180° because both poles will have a 90° phase contribution at ω_{ugb}. So, phase margin is 0° which implies that system is unstable.



If I want to push this ω_{p3} outside your ω_{ugb}, which means this ω_{p2} has to be reduced. And to get 60° phase margin your non-dominant pole should be roughly 1.7 times of your ω_{ugb}.

So, ω_{p3} is now fixed and we cannot change that. Which means your ω_{ugb} should be 1.7 times lesser than ω_{p3}. Now, follow the steps shown in below figure.



So, the total cap required at ω_{p2} is 20 nF and we know that C_{o2} was like order of picoFarads. So, it is negligible. Which means the compensating capacitor (C_C) required is an off-chip cap and you cannot even compensate with the on-chip cap.

So, if we are compensating using the output pole you may require order of microFarad cap because your R_{out} is very small there. So, your capacitor requirement will scale up. But if you compensate at ω_{p2}, then the capacitor requirement will be relatively lower compared to the output pole. So, in this particular case its coming as order of nanofarad.

Let's say you are getting this compensating capacitor as 100 pF or so and with the miller compensation you might get this as 10 pF or so. But even without miller you can compensate it because 100 pF is also possible to put on-chip, but the only thing is your area will be much larger. That's why we go for miller cap to reduce the area.