Power Management Integrated Circuits
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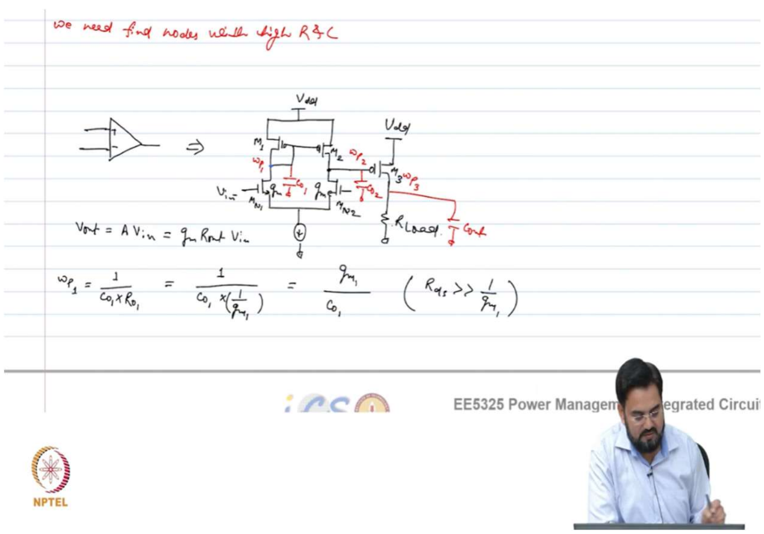
Lecture – 16
Finding the Poles of the Error Amplifier – Part 1

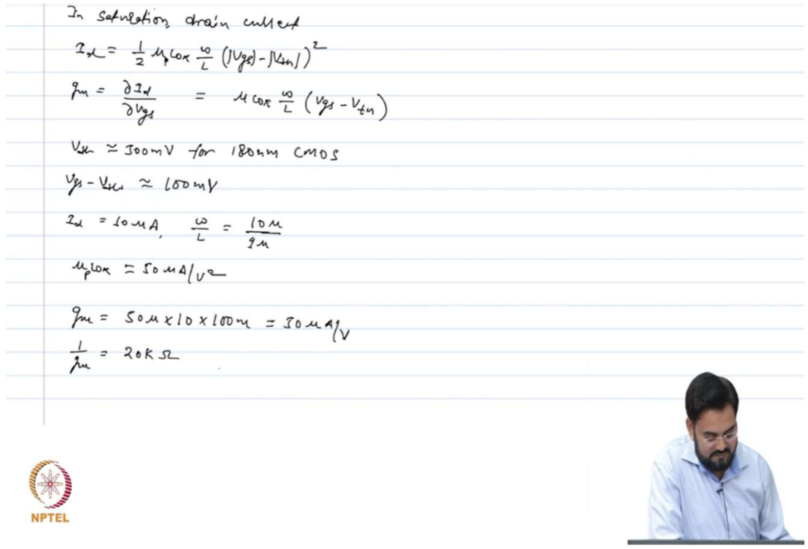
To analyze the stability of a feedback system, first thing we needed to break the loop because we are looking at open loop gain. And then you need to find the poles, and zeros if there are any. In order to find the poles, we need to find the nodes with high R and C because we know that pole $\omega_p = \frac{1}{RC}$.

So, we have a differential pair (single stage op-amp) and at the output of op-amp we have PMOS which is our pass element and it is driving our R_{load} as shown in below figure.



Now we have parasitic capacitances C_{o1} and C_{o2} as shown in above figure. And we have another capacitor which is your C_{out}. So, we are looking at 3 potential nodes which may have poles which fall into within ω_{ugb}. So, $\omega_{p1} = \frac{g_{m1}}{C_{o1}}$.

Now, consider the drain current of MOSFET in saturation region and follow the steps shown in below figure.

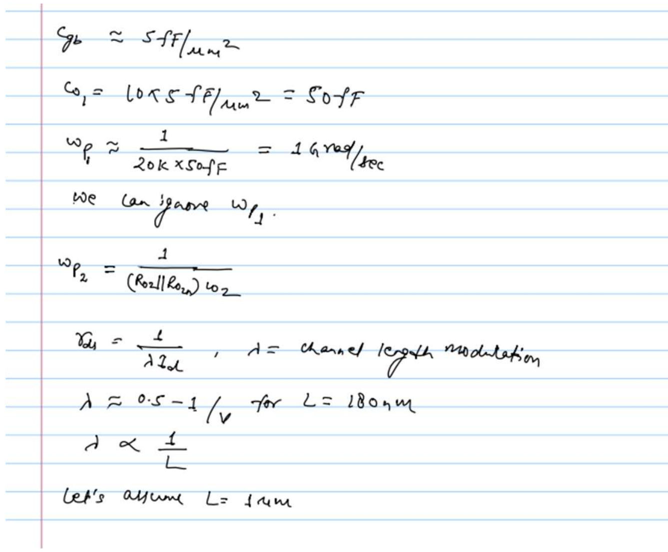


So, V_{th} is approximately 500 mV for 180 nm CMOS process and we usually target overdrive voltage (V_{gs}-V_{th}) of 100 mV. In order to achieve 100 mV overdrive; whatever the bias current you have in one arm of the differential pair and for a particular g_m you can always find the transistor size. For calculations we assumed drain current I_D = 10 μA and assumed other parameters also as shown in above figure and $\frac{1}{g_{m1}}$ turns out to be 20 KΩ.

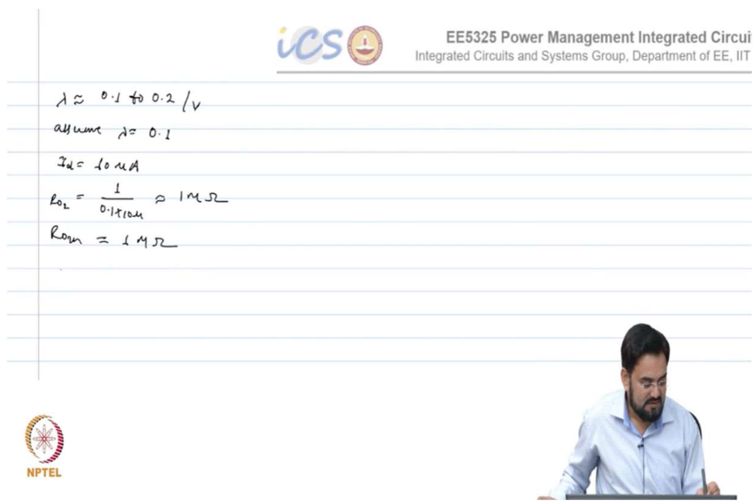
Now, your C_{gb} is roughly 5 fF/μm². If you simulate it will show you as a C_{gg} which is in fact overall gate capacitance. And I am ignoring the overlap capacitance because it is going to be smaller and it is like roughly less than 1 fF. So, your area is 10 μm²; 10 μm is the width and 1 μm is the length. So, C_{o1} is 10 times into 5 which is roughly 50 fF.

So, ω_{p1} turns out to be 1Grad/sec. ($\omega_{p1} = \frac{g_{m1}}{C_{o1}} = \frac{1}{20K \times 50f}$ = 1Grad/sec)

And your ω_{ugb} is not going to be 1 Grad/sec for sure. Mostly it will be order of maximum 10s of MHz not more than that. So, we can ignore ω_{p1}. Now, calculate the second pole which is due to C_{o2}. And R_{out} is coming from R_{ds} of M_2 and M_{n2}.



So, we already considered L = 1 µm for op-amp transistors while calculating g_{m1}. So, for L = 1µm, λ will become approximately 0.1 to 0.2 V^{-1}



So, R_{out} at op-amp output is turns out to be 500 KΩ. By the way this channel length modulation (λ) might be different for PMOS and NMOS, but to simplify the calculation let us assume it is same. But when you start simulating you may get a different number but that is fine. I just want to give you an idea how you find the R_{out} .