Power Management Integrated Circuits
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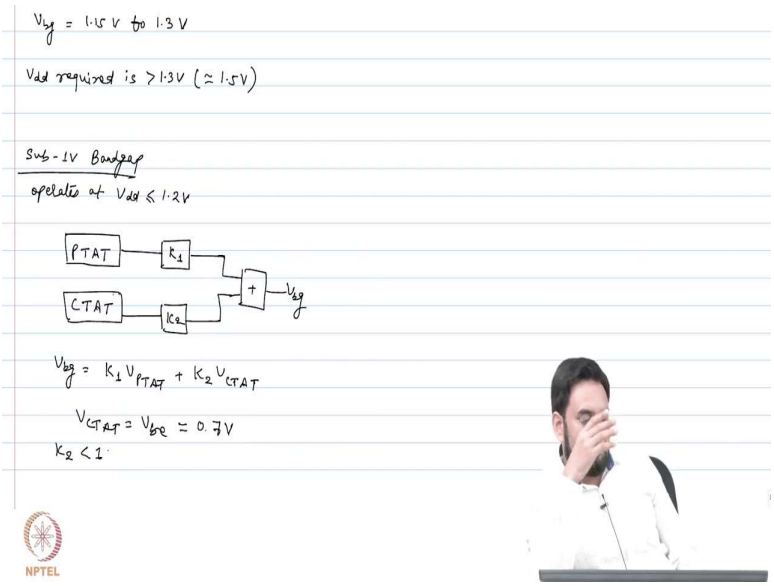
Lecture - 10
Sub-1-volt Bandgap Circuit

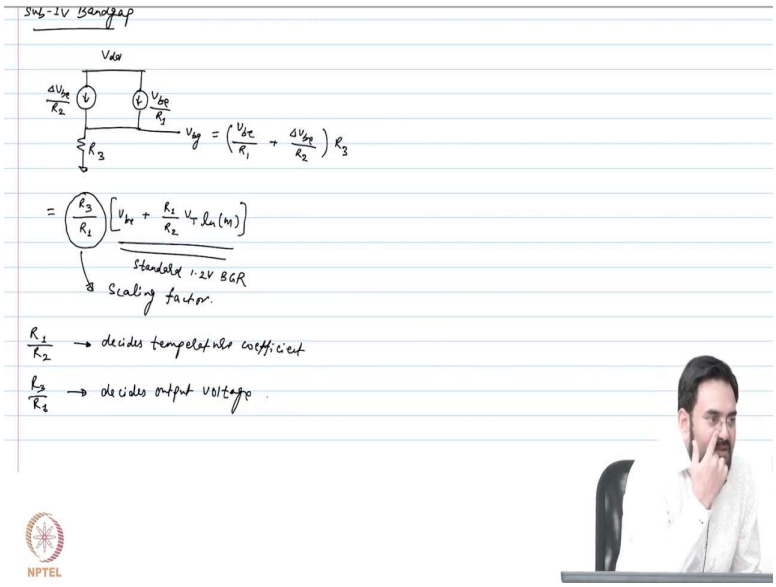
We are getting bandgap voltage (V_{bg}) as 1.15 V to 1.3 V. Which means the V_{dd} required to generate this bandgap is obviously more than 1.3 V. So, V_{dd} required is more than 1.3 V; approximately 1.5 V or so. So, you cannot operate this bandgap below 1.5 V and these days you have 1.2 V devices like in CMOS 65nm. Even 1 V devices you will get as you keep moving into the lower technologies. Which means if I want to design a bandgap which can operate at 1 V or 1.2 V, this circuit will not work because output will be higher than that. That's why we require sub-1 V bandgap. It can be operated at V_{dd} less than or equal to 1.2 V.

So, we need PTAT and CTAT. Now, I will have a scaling factor as shown in below figure and then I will add the two voltages.



If $K_2 < 1$ then you can scale down V_{be}. So, if you choose half then, your PTAT will be added with 0.35 V. Obviously, this voltage will be much lower compared to 1.2 V and you can get the bandgap voltage which is lower than 1 V and which can operate at V_{dd} less than 1.2 V. The most important thing is choosing the K_2, then you choose K_1 accordingly to match the slope.

For sub-1 V bandgap, we have to scale both V_{be} and ΔV_{be}; and add them up as shown in below figure.

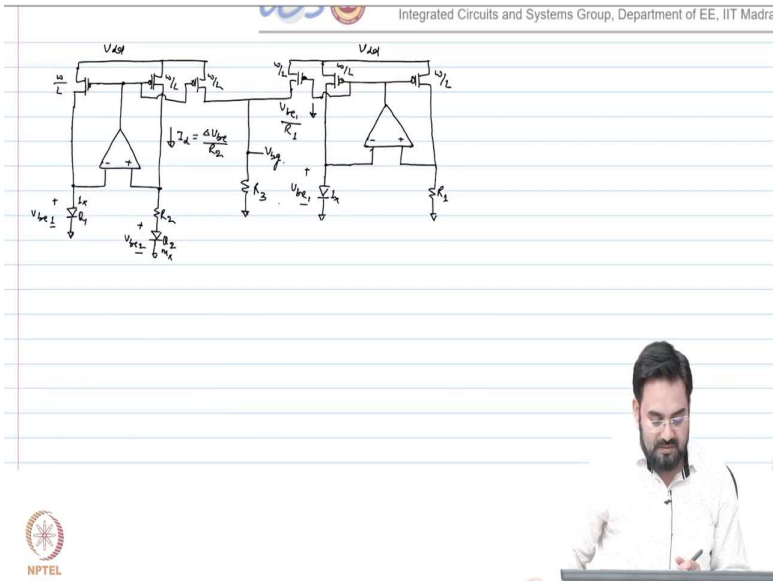


Which means first you choose the ratio of $\frac{R_1}{R_2}$ to cancel the temperature coefficient and then choose $\frac{R_3}{R_1}$ ratio depending upon what value of output voltage you require.

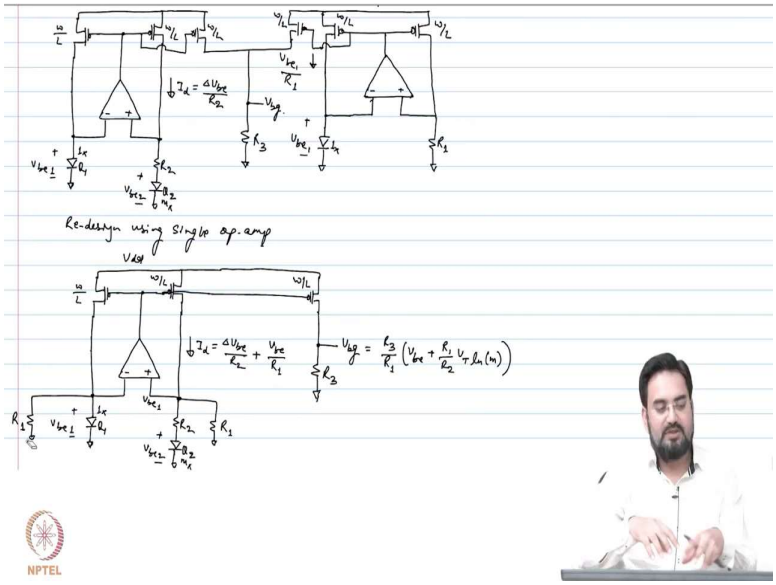
Once you cancelled the temperature coefficient of V_{be} and ΔV_{be}, then you can choose R3 based on what value of output you require. If we make R3 = R1, then we will get our standard bandgap voltage of around 1.2 V.

The circuit diagram for sub-1 V bandgap is shown in below figure. We are dumping the currents $\frac{\Delta V_{be}}{R_2}$ and $\frac{V_{be1}}{R_1}$ into resistor R3 and voltage across R3 gives you bandgap voltage. And we get

$$V_{bg} = \frac{R_3}{R_1}\left(V_{be1} + \frac{R_1}{R_2}\Delta V_{be}\right)$$



We can also design sub-1 V bandgap using a single op-amp as shown in below figure.



Compared to the standard bandgap, do you see any drawback here?

Student: Sir, especially we can see the R_{ds} effect; channel length modulation.

What will happen due to that?

Student: Due to channel length modulation the current will not be exactly matches to that.

So, which means the inaccuracy here might be more compared to the standard bandgap depending upon what V_{bg} you choose. The drain of other two PMOS which are directly connected to the diode side, they are seeing almost same V_{ds} due to negative feedback of the op-amp and the drain voltage is at V_{be1}. So, $V_{ds} = V_{dd} - V_{be1}$. Let's say V_{be1} is roughly 0.7 V and your V_{dd} is 1.2 V. So, both will see V_{ds} of 500 mV.

If your V_{bg} is 0.7 V, then the V_{ds} of current mirror PMOS will be same. But that will also be at one particular temperature because V_{be} is a function of temperature but bandgap voltage is not a function of temperature. So, you might see some variation may be ±100 mV or so. Let's say you designed for V_{bg} of 500 mV, then the V_{ds} of current mirror PMOS device will be much different compared to your V_{ds} of the other two devices.

So, that is why inaccuracy here might be more compared to standard band gap and other thing is now you have to match this R1 also on both sides. So, not only the current mirrors, but these resistors also have to be matched. And R1, R2 is another thing because we want to maintain the ratio; so, they need to be matched. Now we have two R1 resistors here and they have to be perfectly matched. Any mismatch between those resistors will also introduce error in output.

More devices you add, there are more chances of inaccuracy. Because matching the more devices becomes harder compared to fewer devices. Still we get a very decent accuracy with this sub-1 V bandgap. If you are much more concerned about this V_{ds} mismatch then you can always use cascode if you have a larger V_{dd}. With the cascode you can fix that but without cascode there will be some error due to this V_{ds} mismatch. Which means you are forced to use these PMOS sizes; the channel length much larger, so that you can reduce the effect of channel length modulation.