Digital IC Design
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Lecture – 09
Sub-Threshold Leakage

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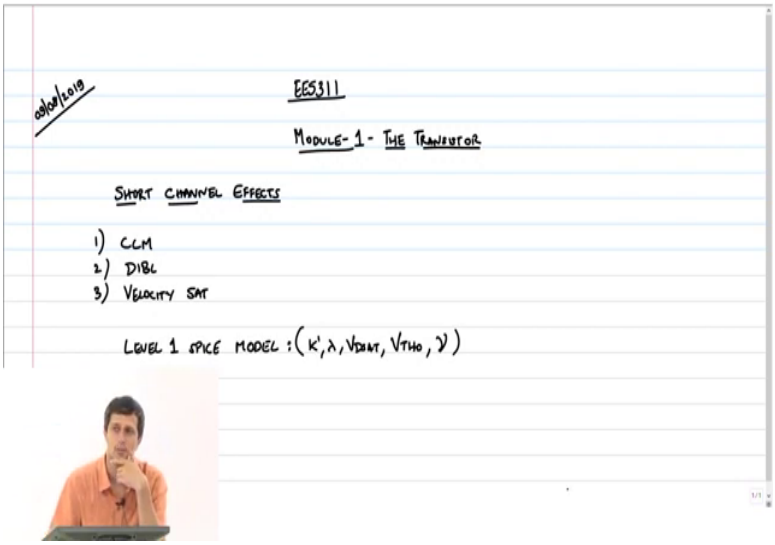

So, let us continue with our discussion on short channel effects. So, we basically did channel length modulation, then we did DIBL, then we did velocity saturation and I believe we stopped with this last class right. So, we modified the equation and we got to the level 1 spice model up right. We derived that and got all the technology parameters out, the 5 parameters right.

The level spice model is characterized by K prime lambda then V DSAT, then V TH naught and gamma. These 5 parameters uniquely characterize the transistor in a particular technology

ok. So, in this class we will move to something very critical and its something that is really plagued the VLSI industry because of scaling ok.

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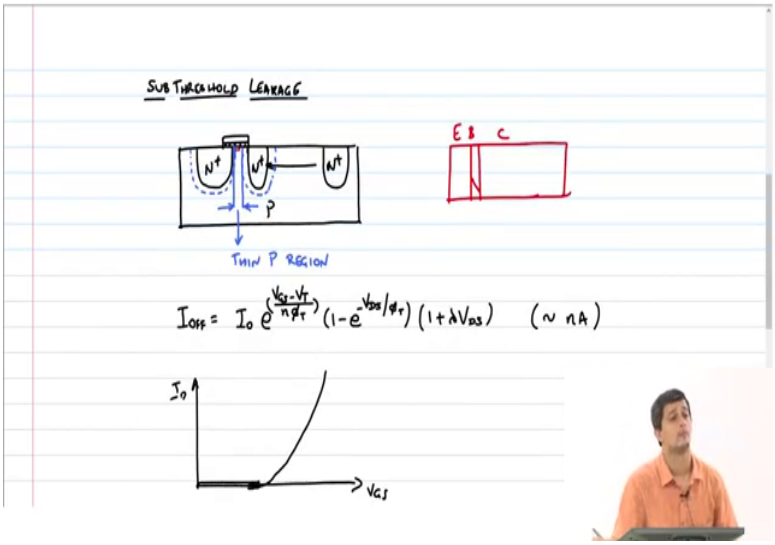

And, this is called sub threshold leakage. So, again if you go back to our picture of the transistor and look at what happens when we bring the drain very close to the source right. Now, the drain that was far away was brought very close and the drain now looks something like this ok; N plus N plus this is P, my gate is now like this ok. So, if you look at this particular structure, it resembles another kind of a device ok. This is a an N plus region, this if you consider you know post the depletion and all that because of the applied potentials; what happens is this becomes a very very very thin region, thin P region ok.

And therefore, this structure now resembles bipolar junction transistor ok. So, what happens is before I actually invert the channel there is there are no free electrons here right. There are

no free electrons in the channel, before I invert there is only excess of holes and this side is N plus, that side is N plus so, really you can have no current flow was the assumption. But, it turns out that if you take a bipolar junction transistor that is like that looks like this, you have an emitter, you have a very thin base emitter, base and collector. Then you could have injection of electrons from this emitter to the collector through that thin base, now this is a property of the base being very very very thin ok.

So, what will happen is you will have some carriers that are just injected across into the base and they sort of by diffusion the concentration will drop exponentially. But, because the base is very thin, the concentration drop will look like a linear region. And, effectively it can go through into the from the base to the collector as well right and that is how you get bipolar junction current by applying potentials.

Here of course, it happens only when there is no channel that is formed. So, again if you come back to our question of does this happen when I turn on the transistor? Yes, it does happen, there is always a diffusion current, there is a drift current. It depends on which current actually dominates in that particular regime, this is not special to only the on state or the off state that I am talking about right.

So, when it is off it is this diffusion current that sort of dominates the transistor, when it is on it is a drift current that dominates the transistor current right. And, not surprisingly because this is like a bipolar junction transistor now, the current I OFF is by the way what was I OFF in our earlier model? 0, right now we are saying that that is not true, it is some current I naught e power V GS minus V T by n phi T into 1 minus e power minus V DS by phi t, phi capital T into 1 plus lambda V DS ok. This is added basically to get continuity in all across all the regimes that is all, right this will not alter the actual value ok.

So, the important part is that my V GS is now going to affect your leakage current exponential and so, will your threshold voltage. So, while you think that it may be good for me to actually reduce the threshold voltage of a transistor and increase the on current, remember that your off current goes up exponentially in that case. So, the gain in the on current is sort of linear or quadratic at most, but the penalty in off current is exponential right.

And, remember as I told you if this is going to happen in 8 billion transistors in your chip then you have a serious problem and especially if it goes up exponentially right.

So, what is the model of a transistor that we envisioned? We said that basically if V GS was 0 or we up to a point right, if you look at your I D versus V GS we wanted the current to be 0 up to some point and then it starts going up right. So, this is what we wanted was an abrupt switch like behavior which means that until it reaches threshold voltage, no current; the moment I exceed the threshold voltage I am able to get a large current. Of course, large depends on whether you are talking of linear saturation, but that current is lean even the linear current is quite high in any case right.

Unfortunately this behavior is obviously not possible, you cannot have such a sharp discontinuity when you are designing devices; in in nature you will never have such discontinuities ok. So, therefore, we need to see how to define this switch like behavior ok. So, what is this switch like behavior that we want? At the threshold voltage when I lower my gate voltage slightly, I want the current to drop significantly right. This is the behavior that I want, but I am not able to achieve it, I have non-ideality. So, we are now going to define something, a particular term that will quantize quantify this idea that we just described ok.

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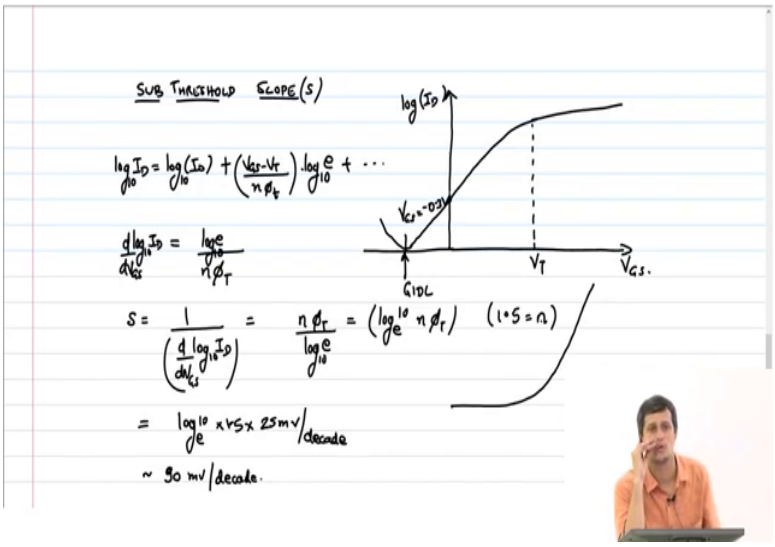

So, that is called sub threshold slope yeah, it is 1 minus e power minus V GS. 1 minus with V GS actually goes up, its a rc charge up yeah. So, first of all if I want to look at the effect of sub-threshold current right, I can now not plot I D versus V GS because, the magnitude of the current isn't going to be nano amperes ok. This the sub threshold equation that we wrote typically will be somewhere in nano amps, let me just write it nano amps.

But obviously, you just made all your calculations now, everything appears in micro amps if you are talking of on correct, linear current saturation it does not matter right. Basically, there is an odd 3 orders of magnitude difference between on current or off current therefore, I cannot plot my I off on, on the linear scale and hope to analyze sub threshold leakage right. Therefore, what do you do? You plot log of I D versus V GS and it turns out that that basically looks like this, remember on the linear scale the same graph looked something like

this. But now, because we are in log I this this change of 1 to 2 micro amps are always just nullified, its basically brought down and it just looks like a very small change.

But, that is actually a very large change because I am plotting log of I D now ok, I am interested in the small changes before the current becomes very large right. So, therefore, if you look at it at V GS equal to 0 right, I do have some off current. This is my maybe let me call it as I OFF 0, the y intercept will tell me what my log of I OFF 0 is ok. There is some non-zero current and now what we are trying to do somewhere here is my V T and the hope is that, if I reduce my V GS slightly below this V T I want the current will drop significantly ok.

So therefore, first let us write down this log of I D equals log of I naught and plus and I will all I will say everything in log to base 10 by the way ok, not long plus V GS minus V T by n phi t into log to base 10 of e plus whatever some other terms that are there. Now, I will differentiate this with respect to V GS d by d V GS of log to base 10 of I D. Everything is a constant, it all vanishes you will get log to base 10 of e divided by n phi t ok. So, now I am going to define my sub threshold slope S as 1 over d by d V GS of log to base 10 of I D.

So, this is what? n phi T by log to base 10 of e or I can just write this as log 10 to base e to n phi T ok. What is n? n is a non-ideality factor even in the p-n junction if you remember you have this the applied potential, if you look at the current it is e power v b i I mean we applied potential divided by n into phi t, that same at non-ideality factor comes. And, that is typically 1.5 for a planar device ok, for a FinFET they are able to bring it down a little bit ok.

So, now we will see what the unit of this particular quantity, sub threshold slope is right. Top n phi T is what? What is the dimension? Volts or I can say milli volts right; so, this is some log to base 10 of e into 1.5 into phi T is about what, at room temperature? 25 millivolts fine right, now since I am doing a log I am going to write this as per decade. So, how much does this come out to be? Can you calculate this? Yeah. How much?

Something, so approximately you should it should come out to be 90 milli volt per decade. So, what does this mean? It means I have to apply 90 milli volts, I have to reduce my gate voltage by 90 milli volt to drop the current by a factor of 10 right. Ideally, I would have liked

to do this with a very very small value, even 10 milli volt I should have been able to drop this to 0 below the threshold voltage, but that is not possible. So, you have a some practical considerations are there and you are limited by this 90 milli volt per decade in planar technologies.

In FinFET technologies people have been able to take this down to about 60 milli volt per decade right. So, the on off you know how good how good the transistor is as a switch will be determined by this particular number ok. Any questions here? So, quite obviously, what happens now by the way if I plot this further here ok, let me let me erase this off. What happens if I lower my V GS? Yeah, I lower V GS below 0 what will happen? Let us look at that equation. So, if that goes below further what will happen? Yeah. It will decrease further right, I keep going what will happen?

So, at some point and other non-ideality kicks in and it will cause this current to go up ok. You can now go and plot this now that you have been shown how to create schematics and do plotting and all you can go do this and see. Plot log I D was V GS sweep it from minus minus 2 to plus 2 volt or minus 1 to plus 1 volt and see what happens. You will see this behavior, the point where this kicks in is called GIDL: Gate Induced Drain Leakage. I will allude to this a little later, just briefly tell you what it is, but the point I am trying to make here is that I cannot keep reducing my V GS.

And, get sub reduce sub threshold leakage more and more and more and more. At some point the drain current starts going up not because of sub threshold leakage, but because of gate induced drain leakage. There is some real tunneling mechanism that happens and therefore, as a designer you should be aware of this point. What is my V GS? Maybe its minus 0.3 volt, below minus 0.3 volt I do not get any gain in taking my V GS, any lower for sub threshold leakage ok. This is what you should keep in mind.