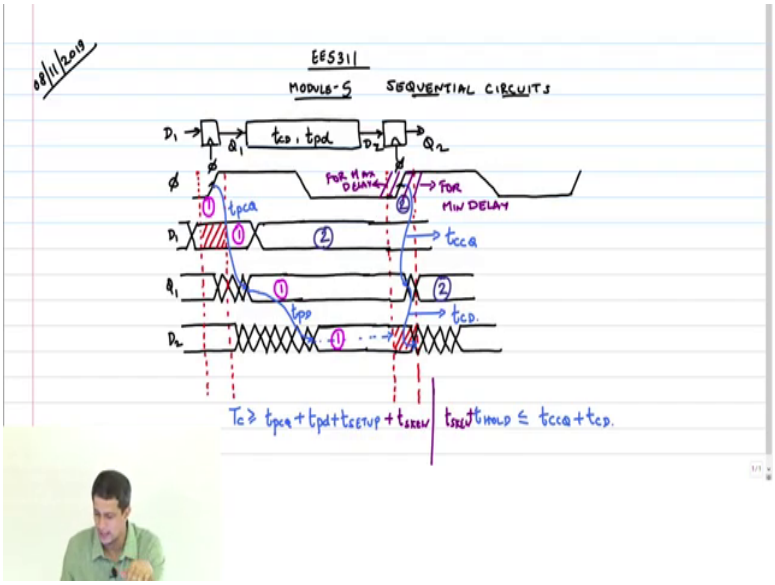
Digital IC Design
Prof. Janakiraman Viraraghavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 75
Flop - Min Delay Constraint

So good morning everyone; let us continue with the discussion on timing analysis ok. So, yesterday there are a lot of people who are not very clear on why they should be a hold violation, ok the diagram probably was not very clear.

(Refer Slide Time: 00:31)



So, I am going to try and explain it by combining the max delay and the min delay waveforms ok; first we will do max delay and then I will show you what will happen in the next cycle ok.

So, that it becomes very clear and also what the problem was we probably did not draw the timing to scale in terms of the contamination delay and the propagation delay right.

The contamination delay can be very small and propagation delay can be quite large; because of this you will see a problem, but let us look at it now ok. So, I have a flop based system like this I am going to draw this small ok, some combinational block like this another clock right.

So, this has a delay of t CD, t p d ok. So, this is D 1, Q 1, D 2 and Q 2 ok. So, we will draw this for across two cycle's fine and then we will see what has to happen. So, my clock basically goes high here ok, phi then my D 1 right is going to make some change sorry here right.

Now, I will also do one more thing, I will mark my setup and whole time windows in red ok. So, you see this, this is my set up time window right, this is my setup and whole time window right where data should not change. Similarly, on the next rising edge you have the same constraint ok, this is my set up time and this is my hold time ok. So, we said now Q 1 right is going to change after the clock right.

So, what will happen is you will find that this Q 1 starts changing here, makes some transitions and then goes like this and its going to remain like that through the entire period ok. D 2, what happens to D 2? It starts changing after some contamination delay and then settles after the propagation delay again right.

So, if you look at this guy, remember this change can happen right here ok. Let me draw this more or less to scale ok, as soon as this Q 1 starts changing, there can be a path in the combinational block which will actually raise to the output. And therefore, you do not have to wait for the propagation delay to finish for the combinational block to start changing, output to start changing ok.

So, therefore, the contamination path can start earlier and then there is going to be Q 2 right of course, Q 2 we do not have to worry, we will have to see when this has to set up ok. So, what is the max delay constraint? This from the clock, it is going to take a delay of t what? t t

pcQ. From this delay it is going to take a delay of what? This t pD and at most right that change has to happen a setup time before right. So, this edge can technically move all the way to here right, that is the worst case constraint right.

So, therefore, we set the max delay constraint is T c should be greater than or equal to t pc Q plus t pd plus t SETUP worst case clear. Now, you look at D 2 ok, this guy has to hold the data, let us assume that this data change, this contamination delay went all the way I mean the propagation delay took it all the way near the setup right clock frequency is very high right. D 2 has to hold this data so, that Q 2 can be sampled correctly right.

So, what is the region in which D 2 should not change? This window right, now once D 1 has been sampled because we have a flop base system there, D 1 is free to change at some point. It need not wait till you know almost the next cycle, it is free to change after what point? After the whole time window, right.

So, again here D is free to change in after this window; it should not change here that is all right; because if it changes in this window then Q 1 will not get sample correctly ok. So, let us assume now D 1 makes a change like this ok, will Q 1 get affected? No, because it is a flop you have passed the sampling edge; when will Q 1 get affected? In the next cycle right so, you come all the way here, let us assume that D 1 is ok. So, I am going to call this event 1 and Q 1 is now working on event 1 this is working on event 1 ok.

Now, you look at D 1 on the next sampling edge right; the moment the clock goes high Q 1 will start changing right and remember it need not wait till right, the moment Q 1 starts changing I told you that D 2 also can start changing. So, if you look at it technically, as soon as this thing start in fact, if you need not even go all the way there; let us probably cause a violation right. D 1 has changed as soon as on the next clock edge. So, this is sampling event 1; this is sampling event 2 right.

I should use a different color may be of color blue, no dark blue event 2 right. So, this is become event 2, Q 1 this is event 2. What has happened now in D 2? Will Q 1 I mean will Q 2 get sample to the value of event 1 or event 2 now? It can be arbitrary right basically,

essentially there is no violation; because the change in D 1 has raced through right and contaminated the value that should have been sampled by the next flop correct.

So, that is why this delay now here if you look at it, this is what? t. What is this delay? t CCQ contamination clock to Q delay. From here there is another contamination delay on the combinational circuit. So, this is t CD right and therefore, what is the constraint in which I mean what is the condition under which this will function correctly, that change in D 2 should happen outside that whole time window right which implies the min delay constraint therefore, is t HOLD should be less than or equal to t CCQ plus t CD.

Now, we said that there can be skew in this and by the way skew is, it is not just the positive edge moves; the entire clock will move, there is a phase shift between these two clocks ok. If only one edge randomly moves which means the time period of that particular thing comes down for that moment right then that is called jitter, that is a random event where one edge can just move like this.

Here the whole clock because of the delay in the clock distribution network right, delay difference in the clock distribution network the whole clock shifts that is Q ok. So now, we basically do you know come and add the condition of skew. So, we say that this clock edge can move like this.

So, for the max delay constraint this is the worst case delay, for max delay this is for ok. And, then you basically go ahead, go ahead and add the constraint of skew into this equation plus t SKEW right and this is t SKEW plus t HOLD should be less than or equal to this. Is this clear? I hope this has made it clear right, you had a question yesterday as to why what is it getting contaminated right.

So, hopefully this picture should make it very clear right. You look at practice drawing these waveforms one after the other, max delay and then you look at the min delay right otherwise you do not know what state the earlier thing was it right. And therefore, you are not sure its actually getting contaminated that is the problem clear. And, also mark this hold setup

window, because next we will go to latch and there its not the rising edge that is going to become your sampling edge, it is a falling edge.

So, you to be very careful so, mark that window very clearly; you should not have a violation in this region, then it will be very clear as to how to obtain the time constraints ok.